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Review Article

FinFETs: From Devices to Architectures

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Since Moore's law driven scaling of planar MOSFETs faces formidable challenges in the nanometer regime, FinFETs and Trigate FETs have emerged as their successors. Owing to the presence of multiple (two/three) gates, FinFETs/Trigate FETs are able to tackle short-channel effects (SCEs) better than conventional planar MOSFETs at deeply scaled technology nodes and thus enable continued transistor scaling. In this paper, we review research on FinFETs from the bottommost device level to the topmost architecture level. We survey different types of FinFETs, various possible FinFET asymmetries and their impact, and novel logic-level and architecture-level tradeoffs offered by FinFETs. We also review analysis and optimization tools that are available for characterizing FinFET devices, circuits, and architectures.

1. Introduction

Relentless scaling of planar MOSFETs over the past four decades has delivered ever-increasing transistor density and performance to integrated circuits (ICs). However, continuing this trend in the nanometer regime is very challenging due to the drastic increase in the subthreshold leakage current (I_{off}) [1–3]. Due to the very narrow channel lengths in deeply scaled MOSFETs, the drain potential begins to influence the electrostatics of the channel and, consequently, the gate loses adequate control over the channel. As a result, the gate is unable to shut off the channel completely in the off-mode of operation, which leads to an increased I_{off} between the drain and the source. The use of thinner gate oxides and high-k dielectric materials helps alleviate this problem by increasing the gate-channel capacitance. However, thinning of gate oxides is fundamentally limited by the deterioration in gate leakage and gate-induced drain leakage (GIDL) [4–6]. Multiple-gate field-effect transistors (MGFETs), which are an alternative to planar MOSFETs, demonstrate better screening of the drain potential from the channel due to the proximity of the additional gate(s) to the channel (i.e., higher gate-channel capacitance) [7–12]. This makes MGFETs superior to planar MOSFETs in short-channel performance metrics, such as subthreshold slope (S), drain-induced barrier lowering (DIBL), and threshold voltage (V_{th}) roll-off. Improvement in these metrics implies less degradation in the transistor's V_{th} with continued scaling, which in turn implies less degradation in I_{off}.

So far, we have referred to planar MOSFETs built on bulk-Si wafers (or bulk MOSFETs) as planar MOSFETs. Fully-depleted silicon-on-insulator (FDSOI) MOSFETs (planar MOSFETs built atop SOI wafers) avoid the extra leakage paths from the drain to source by getting rid of the extra substrate beneath the channel [13, 14]. Their performance metrics are comparable with those of double-gate FETs (DGFETs), which are MGFETs with two gates. Both offer reduced junction capacitance, higher I_{on}/I_{off} ratio, better S, and improved robustness against random dopant fluctuation (RDF). However, DGFETs have a more relaxed constraint on channel thickness, which makes DGFETs more scalable than FDSOI MOSFETs in the long run [15, 16]. Also, DGFET structures can be built on bulk-Si wafers, as well, which makes DGFETs more attractive to foundries that do not want to switch to an SOI process [17, 18].

Among all MGFETs, FinFETs (a type of DGFET) and Trigate FETs (another popular MGFET with three gates) have emerged as the most desirable alternatives to MOSFETs due to their simple structures and ease of fabrication [19–27]. Two or three gates wrapped around a vertical channel enable

easy alignment of gates and compatibility with the standard CMOS fabrication process. In Trigate FETs, an additional selective etching step of the hard mask is involved in order to create the third gate on top of the channel. Although this third gate adds to process complexity, it also leads to some advantages like reduced fringe capacitances and additional transistor width [28–30].

FinFET/Trigate devices have been explored thoroughly in the past decade. A large number of research articles have been published that demonstrate the improved short-channel behavior of these devices over conventional bulk MOSFETs [19–22, 31–33]. Many researchers have presented novel circuit design styles that exploit different kinds of FinFETs [34–48]. Researchers have also explored various symmetric and asymmetric FinFET styles and used them in hybrid FinFET logic gates and memories [49–66]. Newer architectures for caches, networks-on-chip (NoCs), and processors based on such logic gates and memories have also been explored [67–74]. In spite of these advancements in FinFET research, articles that provide a global view of FinFETs from the device level to the topmost architecture level are scarce. Mishra et al. provided such a view at the circuit level [75]. However, FinFETs are not covered at other levels of the design hierarchy. Also, at the circuit level, much progress has been made since the publication of that book chapter. Our article is aimed at a wide range of readers: device engineers, circuit designers, and hardware architects. Our goal is to provide a global view of FinFET concepts spanning the entire IC design hierarchy.

The paper is organized as follows. In Section 2, we review the different types of FinFETs and possible asymmetries that can be designed into their structures. We also discuss the sources of process variations in FinFETs and their impact on FinFET performance. We discuss FinFET process simulation, device simulation, and compact models in Section 3. We describe novel FinFET inverter (INV) and NAND gates, flip-flops, latches, static random-access memory (SRAM), and dynamic random-access memory (DRAM) cells in Section 4. In Section 5, we discuss circuit-level analysis and optimization methodologies and a novel interconnect scheme that leverages FinFETs. We then present a survey of process-voltage-temperature (PVT) variation-aware architecture-level simulation tools in Section 6 and conclude in Section 7.

2. FinFETs

In 1989, Hisamato et al. fabricated a double-gate SOI structure which they called a fully-depleted lean channel transistor (DELTA) [76]. This was the first reported fabrication of a FinFET-like structure. FinFETs have attracted increasing attention over the past decade because of the degrading short-channel behavior of planar MOSFETs [19–24]. Figure 1 demonstrates the superior short-channel performance of FinFETs over planar MOSFETs with the same channel length. Figure 2 shows a conventional planar MOSFET and a FinFET. While the planar MOSFET channel is horizontal, the FinFET channel (also known as the fin) is vertical. Hence, the height

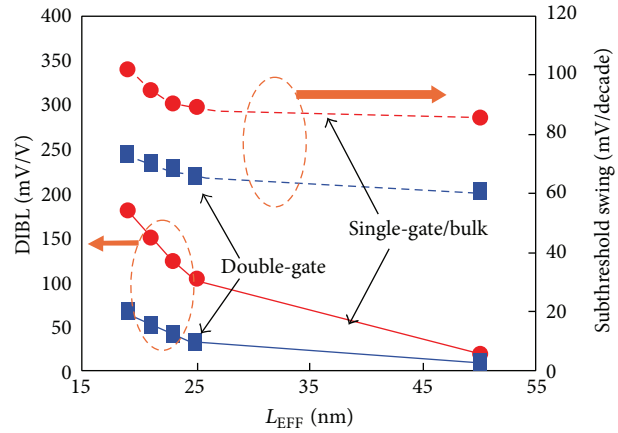

Figure 1: DIBL and subthreshold swing (S) versus effective channel length for double-gate (DG) and bulk-silicon nFETs. The DG device is designed with an undoped body and a near-mid-gap gate material [12].

of the channel (H_{FIN}) determines the width (W) of the FinFET. This leads to a special property of FinFETs known as width quantization. This property says that the FinFET width must be a multiple of H_{FIN}, that is, widths can be increased by using multiple fins. Thus, arbitrary FinFET widths are not possible. Although smaller fin heights offer more flexibility, they lead to multiple fins, which in turn leads to more silicon area. On the other hand, taller fins lead to less silicon footprint, but may also result in structural instability. Typically, the fin height is determined by the process engineers and is kept below four times the fin thickness [77, 78].

Although FinFETs implemented on SOI wafers are very popular, FinFETs have also been implemented on conventional bulk wafers extensively [79–81]. Figure 3 shows FinFETs implemented on bulk and SOI wafers. Unlike bulk FinFETs, where all fins share a common Si substrate (also known as the bulk), fins in SOI FinFETs are physically isolated. Some companies prefer the bulk technology because it is easier to migrate to bulk FinFETs from conventional bulk MOSFETs. However, FinFETs on both types of wafers are quite comparable in terms of cost, performance, and yield, and it is premature to pick a winner. From this point on, our discussion will be limited to SOI FinFETs unless otherwise mentioned.

Trigate FETs, referred to interchangeably as FinFETs, in this paper so far, are a variant of FinFETs, with a third gate on top of the fin. Intel introduced Trigate FETs at the 22 nm node in the Ivy-Bridge processor in 2012 [28, 82]. Figure 4 shows a Trigate FET along with a FinFET. The thickness of the dielectric on top of the fin is reduced in Trigate FETs in order to create the third gate. Due to the presence of the third gate, the thickness of the fin also adds to the channel width. Hence, Trigate FETs enjoy a slight width advantage over FinFETs. Trigate FETs also have less gate-source capacitance compared to FinFETs due to additional current conduction at the top surface, but this advantage is diminished by increased parasitic resistance [29].

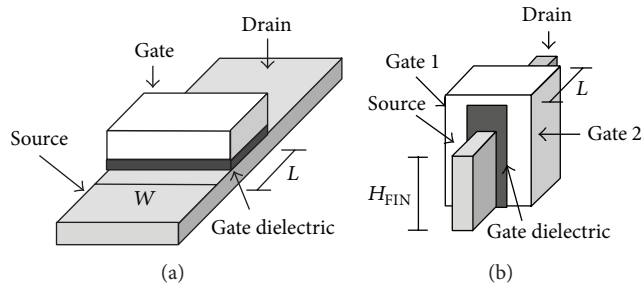

Figure 2: Structural comparison between (a) planar MOSFET and (b) FinFET.

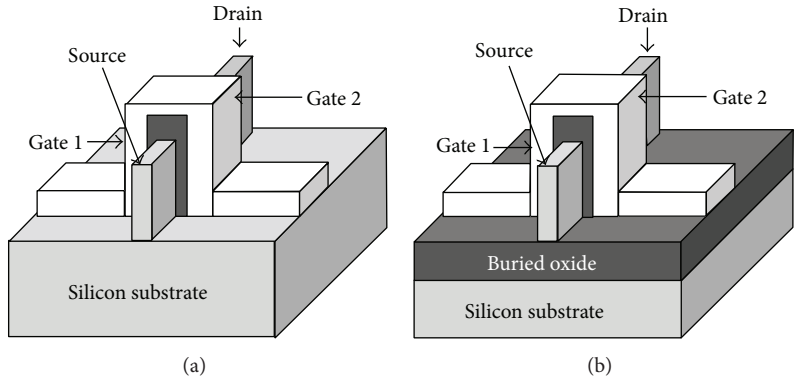

Figure 3: Structural comparison between (a) bulk and (b) SOI FinFETs.

Yang and Fossum compared Trigate FETs and FinFETs and argued that FinFETs are superior to Trigate FETs in the long run [83]. They showed that although undoped Trigate FETs may enjoy more relaxed body thickness, they are not competitive with FinFETs in SCE metrics. When trying to achieve comparable SCE metrics, Trigate FETs lose the scaling advantage and suffer from significant layout area disadvantage. However, like the bulk versus SOI debate, it is also premature to declare a clear winner between FinFETs and Trigate FETs. From this point onwards, we will consider FinFETs only unless stated otherwise.

FinFETs can be fabricated with their channel along different directions in a single die. Fabrication of planar MOSFET channels along any crystal plane other than ⟨100⟩ is difficult due to process variations and interface traps [36, 84]. However, FinFETs can be fabricated along the ⟨110⟩ plane as well. This results in enhanced hole mobility. ⟨110⟩-oriented FinFETs can be fabricated by simply rotating the transistor layout by 45° in the plane of a ⟨100⟩ wafer [85]. Thus, nFinFETs implemented along ⟨100⟩ and pFinFETs along ⟨110⟩ lead to faster logic gates since this gives designers an opportunity to combat the inherent mobility difference between electrons and holes. However, this multiorientation scheme has an obvious drawback of increased silicon area [85]. In the following sections, we discuss FinFET classifications and process variations in detail.

2.1. FinFET Classification. There are two main types of FinFETs: shorted-gate (SG) and independent-gate (IG). SG FinFETs are also known as three-terminal (3T) FinFETs and IG FinFETs as four-terminal (4T) FinFETs. In SG FinFETs, both the front and back gates are physically shorted, whereas in IG FinFETs, the gates are physically isolated (Figure 5). Thus, in SG FinFETs, both gates are jointly used to control the electrostatics of the channel. Hence, SG FinFETs show higher on-current (I_{on}) and also higher off-current (I_{off} or the subthreshold current) compared to those of IG FinFETs. IG FinFETs offer the flexibility of applying different signals or voltages to their two gates. This enables the use of the back-gate bias to modulate the V_{th} of the front gate linearly. However, IG FinFETs incur a high area penalty due to the need for placing two separate gate contacts.

SG FinFETs can be further categorized based on asymmetries in their device parameters. Normally, the workfunctions (Φ) of both the front and back gates of a FinFET are the same. However, the workfunctions can also be made different. This leads to an asymmetric gate-workfunction SG FinFET or ASG FinFET (Figure 6) [86, 87]. ASG FinFETs can be fabricated with selective doping of the two gate-stacks. They have very promising short-channel characteristics and have two orders of magnitude lower I_{off} compared to that of an SG FinFET, with I_{on} only somewhat lower than that of an SG FinFET [49]. Figures 7 and 8 show comparisons of the drain current I_{DS} versus front-gate voltage V_{GFS} curves for SG, IG, and ASG nFinFETs and pFinFETs, respectively, demonstrating the advantages of ASG FinFETs.

Apart from gate-workfunction asymmetry, other asymmetries have also been explored in FinFETs. Goel et al. [57] show that asymmetric drain-spacer-extended (ADSE)

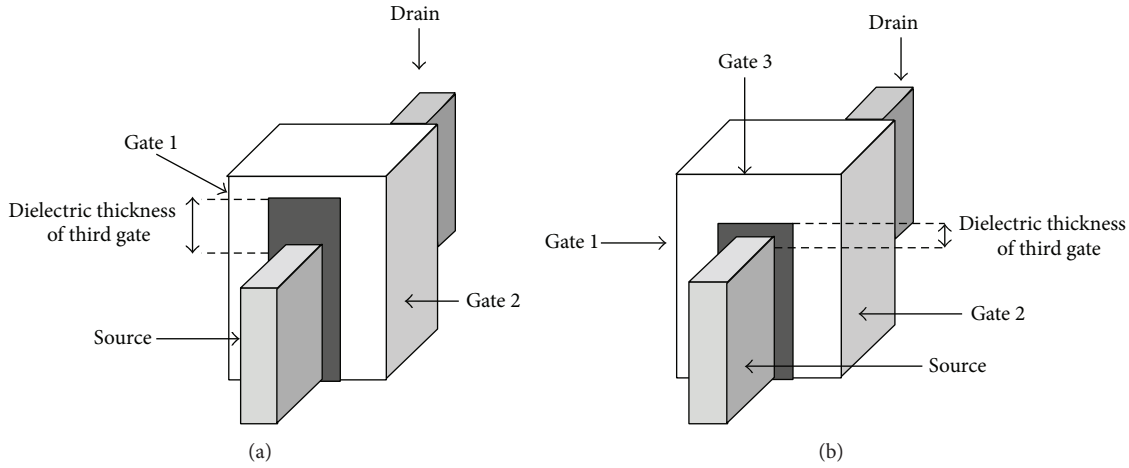

Figure 4: Structural comparison between (a) FinFET and (b) Trigate FET.

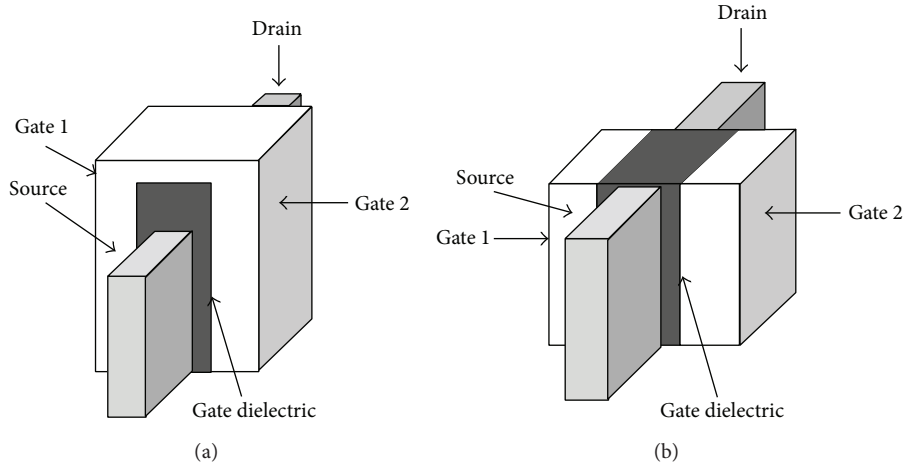

Figure 5: Structural comparison between (a) SG and (b) IG FinFET.

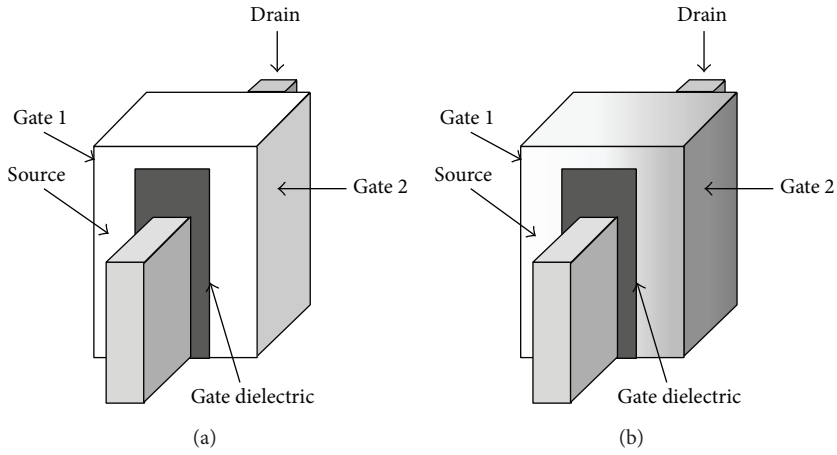

Figure 6: Structural comparison between (a) SG and (b) ASG FinFET; shaded gate implies different workfunctions.

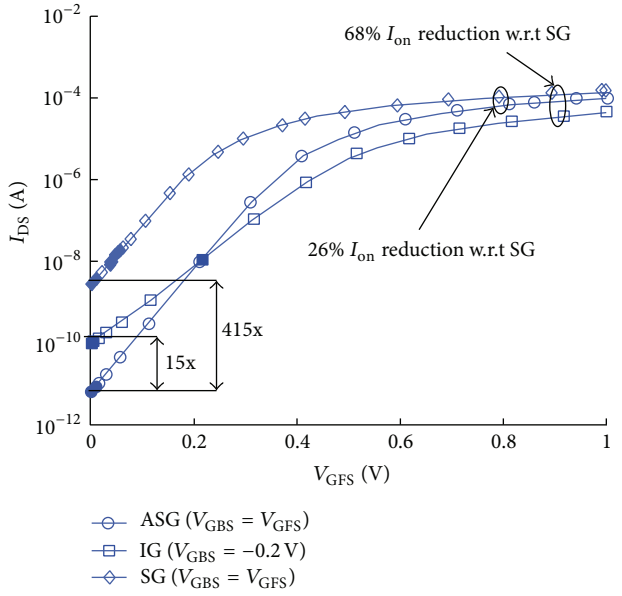

FIGURE 7: Drain current (I_{DS}) versus front-gate voltage (V_{GFS}) for three nFinFETs [49].

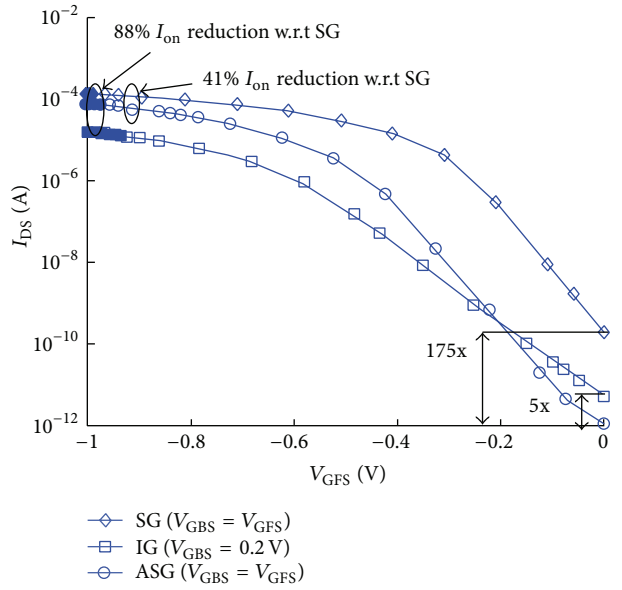

FIGURE 8: Drain current (I_{DS}) versus front-gate voltage (V_{GFS}) for three pFinFETs [49].

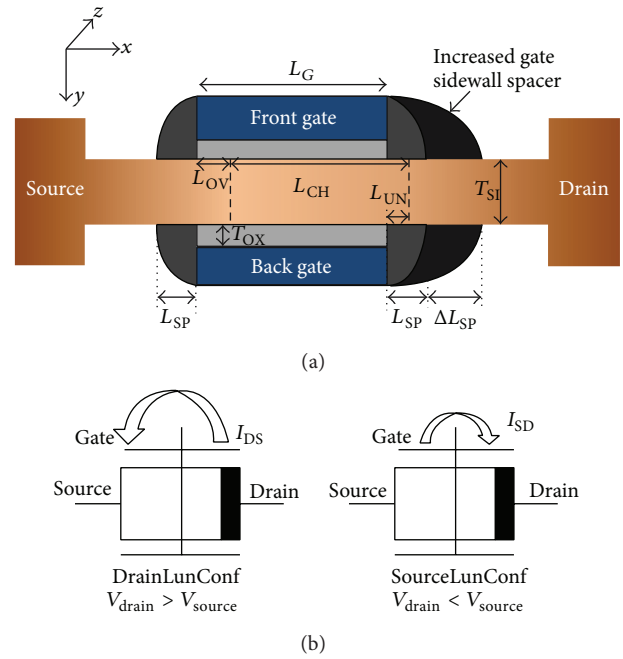

FIGURE 9: Asymmetric drain spacer extension (ADSE) FinFET [57].

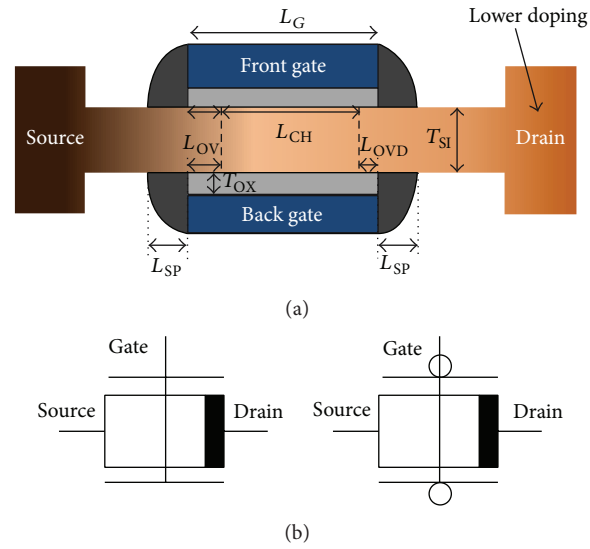

FIGURE 10: Asymmetric drain-source doped (AD) FinFET [58].

FinFETs (Figure 9) can lead to improved short-channel characteristics because of an indirect increase in channel length. However, this improvement comes at the cost of an increased layout area. This asymmetry also destroys the conventional interchangeable source-drain concept in CMOS. An asymmetry is created in the drain-to-source current I_{DS} and source-to-drain current I_{SD} because of the extra underlap. This asymmetry affects FinFET pass transistor performance. Asymmetric drain-source doped (AD) FinFETs (Figure 10), with an order of magnitude difference in the drain and source doping concentrations, have been exploited in [58]. This also destroys the conventional symmetry in I_{DS} and I_{SD}, which again leads to asymmetric FinFET pass transistor performance. SCEs are improved in AD FinFETs because of lower electric fields in the lower-doped drain. FinFETs with asymmetric oxide thickness (ATox) (Figure 11) have also been proposed [88, 89]. Such FinFETs have good subthreshold slopes. Use of IG FinFET (or 4T FinFET) in this context also enables variable V_{th}'s. This asymmetry can be achieved using a ion-bombardment-enhanced etching process. Finally, asymmetric fin-height FinFETs have also been explored [61, 90]. Since the channel width of a FinFET is proportional to

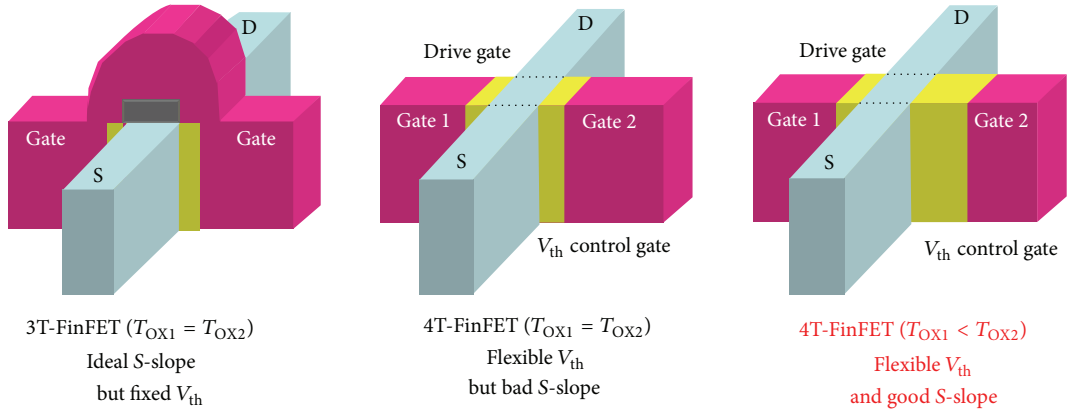

Figure 11: Asymmetric oxide thickness (ATox) FinFET [89].

Table 1: 22 nm SOI FinFET parameter values.

L_{GF}, L_{GB} (nm)	24
Effective T_{OXF}, T_{OXB} (nm)	1
T_{SI} (nm)	10
H_{FIN} (nm)	40
H_{GF}, H_{GB} (nm)	10
L_{SPF}, L_{SPB} (nm)	12
L_{UN} (nm)	4
N_{BODY} (cm^{-3})	10^{15}
$N_{S/D}$ (cm^{-3})	10^{20}
Φ_{GF}, Φ_{GB} (eV)	4.4(n), 4.8(p)
FP (nm)	50
GP (nm)	92

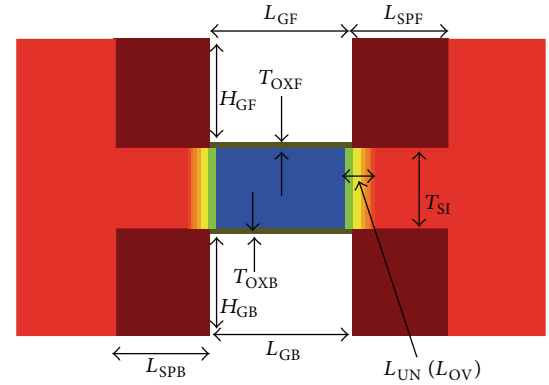

Figure 12: A 2D cross-section of a 3D nFinFET with extended source and drain [49].

its fin height, pFinFETs with taller fins can compensate for the inherent mobility mismatch between electrons and holes.

Figure 12 shows a two-dimensional (2D) cross-section of a three-dimensional (3D) FinFET, illustrating various device parameters of interest. Typical values for these parameters are given in Table 1. L_{GF}, L_{GB}, T_{OXF}, T_{OXB}, T_{SI}, H_{FIN}, H_{GF}, H_{GB}, L_{SPF}, L_{SPB}, L_{UN}, N_{BODY}, $N_{S/D}$, Φ_{GF}, Φ_{GB}, FP, and GP refer to the physical front- and back-gate lengths, front- and back-gate effective oxide thicknesses, fin thickness, fin height, front- and back-gate thicknesses, front- and back-gate spacer thicknesses, gate-drain/source underlap, body doping, source/drain doping, front- and back-gate workfunctions, fin pitch, and gate pitch, respectively.

2.2. Process Variations. Reduced feature size and limited photolithographic resolution cause statistical fluctuations in nanoscale device parameters. These fluctuations cause variations in electrical device parameters, such as V_{th}, I_{on}, I_{off}, and so forth, known as process variations. These variations can be inter-die or intra-die, correlated or uncorrelated, depending on the fabrication process. They lead to mismatched device strengths and degrade the yield of the entire die. This is why continued scaling of planar MOSFETs has become so difficult.

In planar MOSFETs, a sufficient number of dopants must be inserted into the channel in order to tackle SCEs. However, this means that RDF may lead to a significant variation in V_{th}. For example, at deeply scaled nodes, the $3(\sigma/\mu)$ variation in V_{th} caused by discrete impurity fluctuation can be greater than 100% [91]. Since FinFETs enable better SCE performance due to the presence of the second gate, they do not need a high channel doping to ensure a high V_{th}. Hence, designers can keep the thin channel (fin) at nearly intrinsic levels ($10^{15} cm^{-3}$). This reduces the statistical impact of RDF on V_{th}. The desired V_{th} is obtained by engineering the workfunction of the gate material instead. Low channel doping also ensures better mobility of the carriers inside the channel. Thus, FinFETs emerge superior to planar MOSFETs by overcoming a major source of process variation.

FinFETs do suffer from other process variations. Due to their small dimensions and lithographic limitations, FinFETs are subjected to several important physical fluctuations, such as variations in gate length (L_{GF}, L_{GB}), fin-thickness (T_{SI}), gate-oxide thickness (T_{OXF}, T_{OXB}), and gate underlap (L_{UN}) [91–97]. For example, gate oxide is on the etched sidewall of the fin, and may suffer from nonuniformity. The degree of nonuniformity depends on the line-edge roughness (LER) of the fin. LER also causes variations in fin thickness.

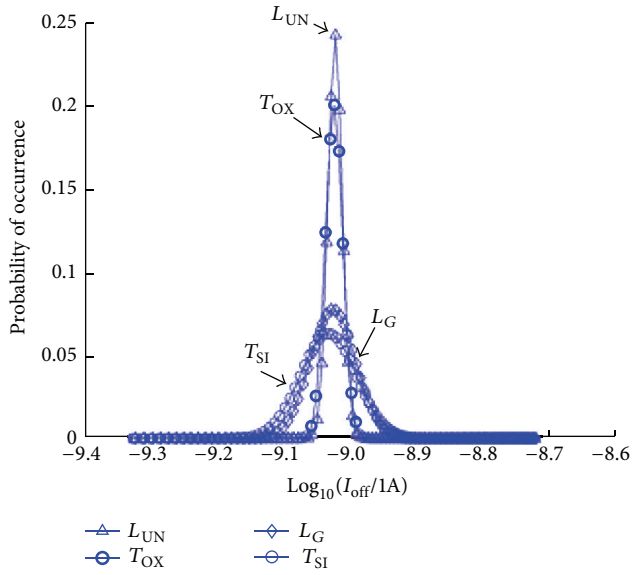

FIGURE 13: Distribution of leakage current (I_{off}) for different process parameters, each varying independently [94].

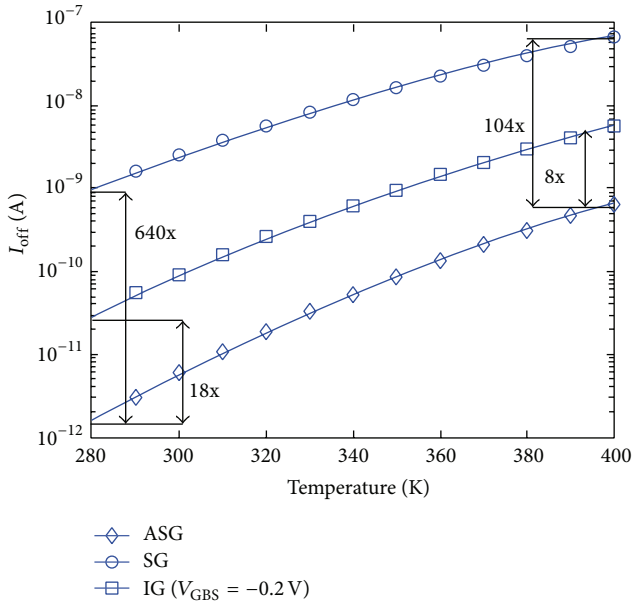

FIGURE 14: I_{off} versus temperature for three nFinFETs [49].

Figure 13 shows the impact of parametric variations on the subthreshold current (I_{off}) of an nFinFET. Xiong and Bokor have studied the sensitivity of electrical parameters to various physical variations in devices designed with a nearly intrinsic channel [91].

Choi et al. have studied temperature variations in FinFET circuits under above-mentioned physical parameters variations [98]. They showed that even under moderate process variations ($3(\sigma/\mu)$ = 10%) in gate length (L_{GF}, L_{GB}) and body thickness (T_{SI}), thermal runaway is possible in more than 15% of ICs when primary input switching activity is 0.4. The effect of temperature variation is more severe in

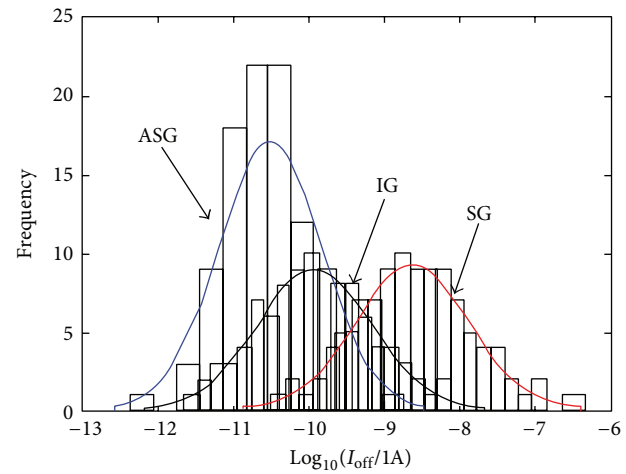

FIGURE 15: Distributions of I_{off} under process variations for three nFinFETs [49].

SOI FinFETs because the oxide layer under the fin has poor thermal conductivity. Hence, heat generated in the fin cannot dissipate easily in SOI FinFETs. Bhoj and Jha have evaluated SG, IG, and ASG FinFETs under temperature variation and found that even though I_{off} degrades for all three FinFETs at a higher temperature, ASG FinFETs still remain the best and retain a 100× advantage over SG FinFETs, as shown in Figure 14 [49]. They also showed the distribution of I_{off} under process variations for the three FinFETs (Figure 15).

3. FinFET Device Characterization

In this section, we discuss various ways of characterizing FinFET devices through simulation. Process simulation followed by device simulation constitutes a technology computer-aided design (TCAD) characterization flow of nanoscale devices, such as FinFETs. Compact models, on the other hand, have been another very popular way of characterizing CMOS devices for decades.

3.1. Process Simulation. Real devices undergo several processing steps. The functionality and performance of the fabricated devices depend on how optimized the process flow is. TCAD process simulation is, therefore, an important step in FinFET device optimization. Process simulation is followed by device simulation. These two simulation steps form an optimization loop in which small changes in the process flow (e.g., time, temperature, doses, etc.) can lead to desirable electrical characteristics of the device. Thus, process simulation helps device engineers explore the parameter space of the process, obviating the need for actual device fabrication. Although 3D process simulation is computationally very expensive, it not only gives good insights into device physics but also provides a cost-effective pre-fabrication process optimization flow.

The Sentaurus process and device simulator from Synopsys is a widely used tool for process simulation [99]. Its 3D process simulation framework is compatible with the mainstream 2D TCAD framework TSUPREM4/MEDICI

(also from Synopsys). The 2D framework has been used by designers over the past decade and has been well-calibrated with advanced CMOS libraries. Nawaz et al. have implemented a complete FinFET process flow as a commercially-available process and device simulation environment [100]. As in real devices, all important geometrical features, such as corner roundings and 3D facets, have been implemented in their setup.

Process simulations of large layouts that consist of multiple devices incur extremely high computational costs. A novel layout/process/device-independent TCAD methodology was proposed in [54] in order to overcome the process simulation barrier for accurate 3D TCAD structure synthesis. In it, Bhoj et al. adopt an automated structure synthesis approach that obviates the need for repetitive 3D process simulations for different layouts. In this approach, process-simulated unit devices are placed at the device locations in the layout, eliminating the need for process simulation of the entire layout, thereby reducing computational costs significantly. This structure synthesis approach, followed by transport analysis based capacitance extraction methodology, has been shown to capture accurate parasitic capacitances in FinFET SRAMs and ring oscillators in a practical timeframe [54, 55, 63, 66]. Accurate extraction of parasitic capacitances has led to a comprehensive evaluation of transient metrics of various FinFET SRAM bitcells [55].

3.2. Device Simulation. After process simulation generates a meshed device structure, device simulation is performed on the structure by invoking appropriate transport models. The conventional drift-diffusion transport model is not adequate for capturing SCEs in nanometer MOSFETs and FinFETs. The hydrodynamic model, with quantum corrections (such as density gradient models), has been popular among researchers for FinFET device simulation [101]. Other more accurate models, such as Green's function based solution to Boltzmann's transport equation, impose a drastic computational burden [101]. In order to simulate circuits with multiple devices, Sentaurus device (Synopsys) allows mixed-mode device simulation. Here, individual FinFET devices are connected externally using wires or other circuit elements to form a netlist and coupled transport equations are solved on the entire netlist. This feature enables device engineers to see how the device behaves when used in a circuit.

3.3. Compact Models. Physics based compact models of FinFETs have been a very useful tool for designers. Berkeley short-channel IGFET model (BSIM) and University of Florida double-gate model (UFDG) for SOI multigate MOSFETs and FinFETs were built using TCAD and calibrated using fabricated hardware [102–105]. These models are compatible with commercial circuit simulators, such as simulation program with integrated circuit emphasis (SPICE). Hence, large netlists can be simulated with these models as long as the solution space is within their range. However, device simulation precedes derivation of compact models and is more accurate. Thus, all results presented in this article are based on mixed-mode device simulations.

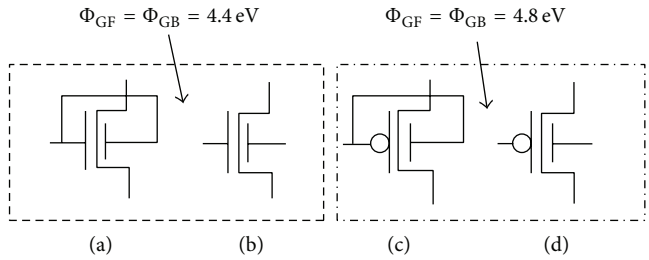

Figure 16: Schematic diagrams of (a) SG nFinFET, (b) IG nFinFET, (c) SG pFinFET, and (d) IG pFinFET. Their gate workfunctions are also shown [49].

4. FinFET Standard Cells

After the characterization of individual n/pFinFET devices, we move one level up to characterization of FinFET logic gates, latches, flip-flops, and memory cells, which are the building blocks of any digital integrated circuit [49–51]. IG and ASG FinFETs offer new leakage-delay tradeoffs in FinFET logic gates that can be exploited in low-power or high-performance applications. The schematic diagrams of SG and IG FinFETs are shown in Figure 16. Schematic diagrams of ASG FinFETs are shown in Figure 17. Bhoj and Jha have performed an in-depth analysis and comparison of SG, IG, and ASG FinFET based INV and NAND2 (two-input NAND) gates [49]. These two gates are the most essential building blocks of any logic library because any logic network can be built with just these two gates.

4.1. SG/IG INV. There are four possible configurations of an INV based on how SG and IG FinFETs are combined to implement them. They are called SG, low-power (LP), IGn, and IGp INV. Their schematic diagrams are shown in Figure 18. As suggested by its name, an SG INV has SG n/pFinFETs. It has a highly compact layout. The other three configurations use at least one IG FinFET. The back-gate of an IG pFinFET (nFinFET) is tied to a V_{HIGH} (V_{LOW}) signal. When these signals are reverse-biased, for example, when V_{HIGH} is 0.2 V above V_{DD} and V_{LOW} is 0.2 V below ground, there is a significant reduction in I_{off}. The presence of an IG FinFET also leads to a more complex layout, resulting in 36% area overhead relative to that of an ×2 SG INV (that is double the size of a minimum-sized SG INV). Table 2 compares the normalized area, delay, and leakage of the various INVs. Clearly, SG INV is the best in area and propagation delay (T_p), but incurs much higher leakage current than LP INV. However, LP INV performs poorly in area and propagation delay. IGn INV, however, looks promising based on its intermediate area, delay, and leakage.

4.2. SG/IG NAND2. Similar to INVs, NAND2 gates also have SG (LP) configurations in which all transistors are SG (IG) FinFETs. Since there are more transistors in a NAND2 gate than in an INV, there are more opportunities available for combining SG and IG FinFETs. This leads to various other configurations: MT, IG, IG2, XT, and XT2. Schematic

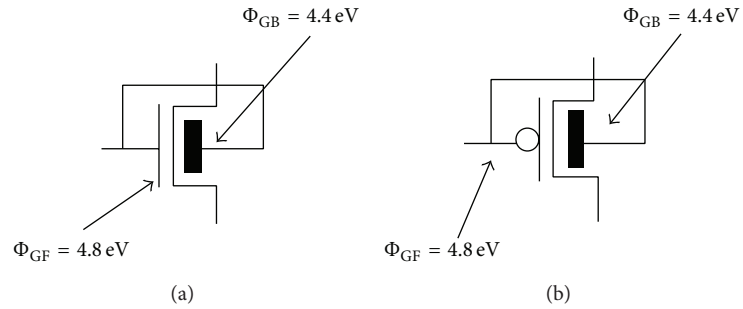

Figure 17: Schematic diagrams of ASG: (a) nFinFET and (b) pFinFET. Their gate workfunctions are also shown [49].

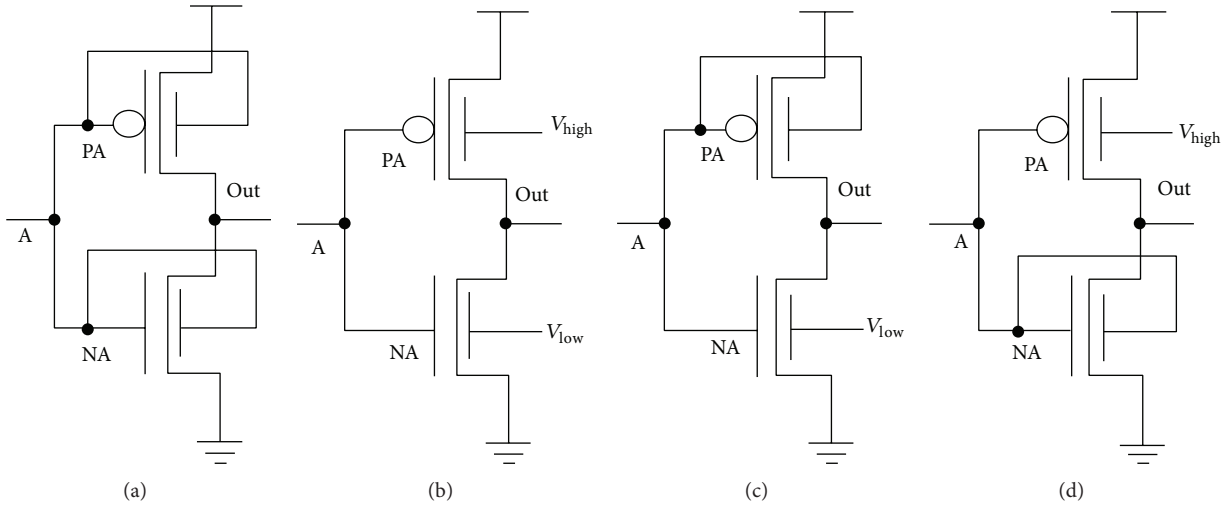

Figure 18: Schematic diagrams of (a) SG INV, (b) LP INV, (c) IGn INV, and (d) IGp INV [49].

Table 2: Comparison of FinFET INVs [49].

Topology	SG	LP	IGn	IGp
Area	1	1.36	1.36	1.36
Avg. I_{off}	20.92	1	2.75	19.25
T_p	1	3.67	1.67	2.92

Table 3: Comparison of FinFET NAND2 gates [49].

Topology	SG	LP	MT	IG	IG2	XT	XT2
Area	1	1.27	1.27	1	1	1.27	1
Avg. I_{off}	18.40	1	7.00	18.40	7.73	18.13	7.73
T_p (Toggle A)	1	4.13	3.80	1.60	2.08	3.20	1.47
T_p (Toggle B)	1	4.50	3.88	1.69	2.02	3.58	1.38
T_p (Toggle AB)	1	3.48	3.09	1	1.55	2.38	1.55

diagrams of SG, LP, and MT NAND2 gates are shown in Figure 19. Schematic diagrams for IG, IG2, XT, and XT2 NAND2 gates are shown in Figure 20. Table 3 shows the normalized area, delay, and leakage of all these NAND2 gates. Again, all comparisons in Table 3 are made relative to ×2 SG NAND2 gate, because it is the largest SG NAND2 gate that can be accommodated in the standard cell height. SG NAND2 outperforms others in area and propagation delay, but consumes significantly more leakage current than LP NAND2. Out of all the variants, XT2 NAND2 stands out as a reasonable compromise.

4.3. ASG Logic Gates. Bhoj and Jha investigated INV and NAND2 gates with a mix of SG and ASG FinFETs [49]. Schematics/layouts of any SG-FinFET logic gate can be converted to those of an ASG-FinFET logic gate, as shown in Figure 21, without any area overhead. Hence, introduction of ASG FinFETs only impacts leakage and propagation delay. Preserving some of the SG FinFETs in the NAND2S gate (Figure 21(c)) enables leakage-delay tradeoffs, as evident from the leakage-delay spectrum shown in Figure 22 for various logic gates. The pure ASG gates lie in the left half of the spectrum, indicating low leakage, while pure SG gates lie in the bottom half of the spectrum, indicating less delay.

4.4. SG/IG/ASG Latches and Flip-Flops. Brute-force transmission gate (TG) and half-swing (HS) latches and flip-flops (as shown in Figures 23 and 24) implemented with SG, IG, and ASG FinFETs have also been investigated [49, 50]. Tawfik et al. proposed an IG latch by introducing IG FinFETs in the feedback inverter (I3) of the all-SG TG latch in Figure 23(a).

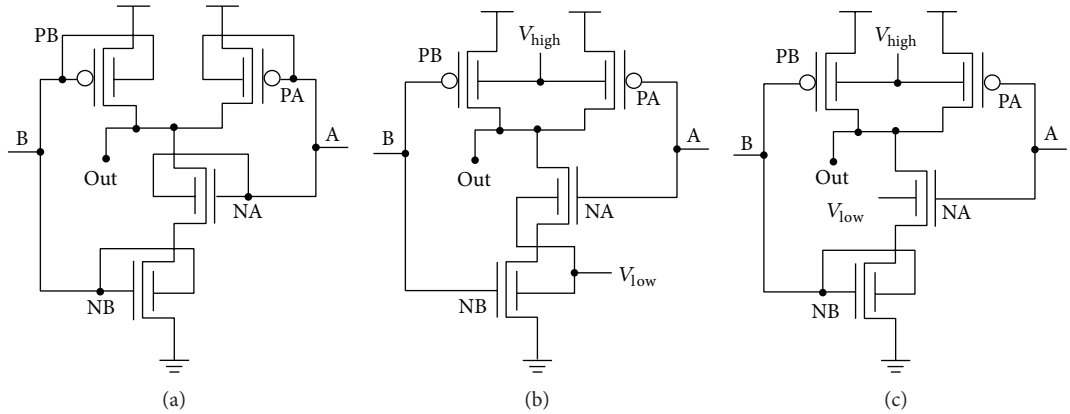

Figure 19: Schematic diagrams of NAND2 gates: (a) SG, (b) LP, and (c) MT [49].

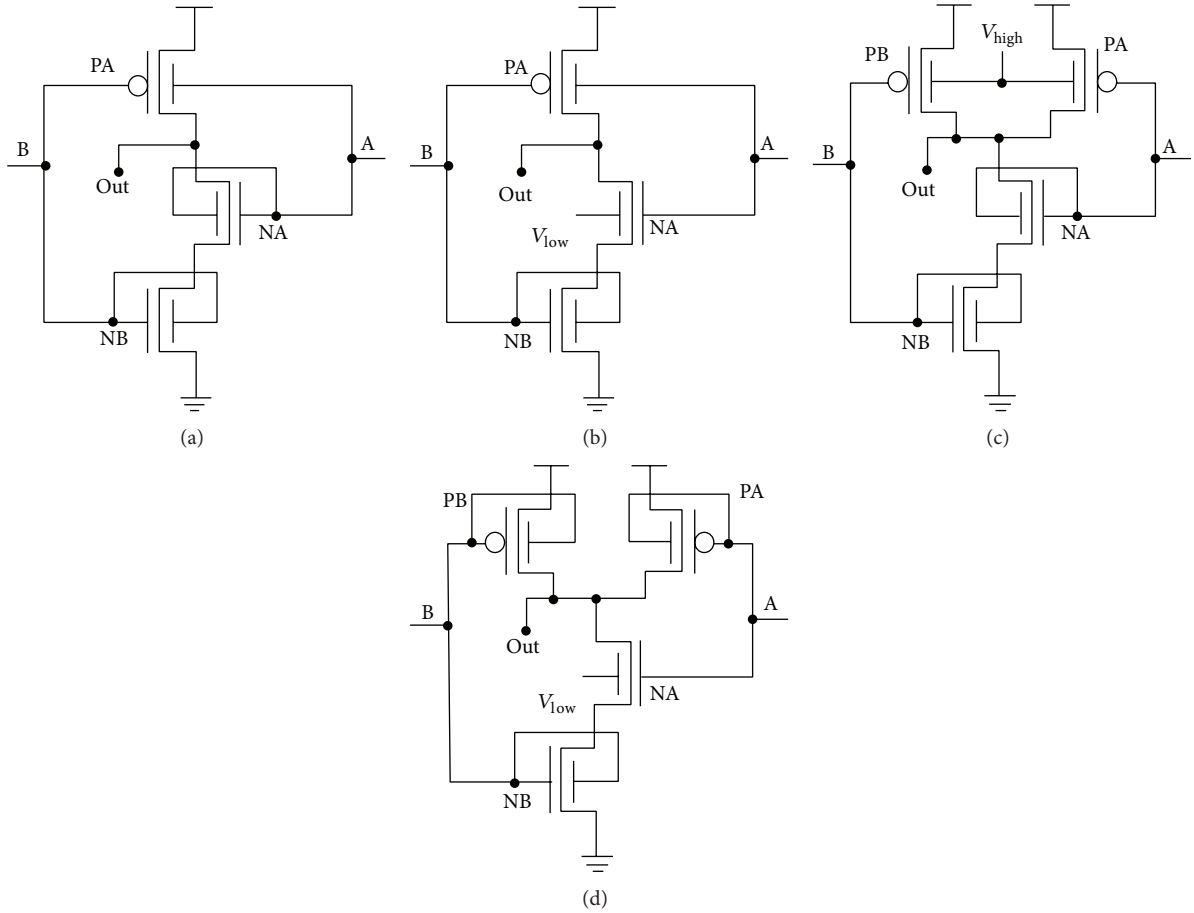

Figure 20: Schematic diagrams of NAND2 gates: (a) IG, (b) IG2, (c) XT, and (d) XT2 [49].

With appropriate reverse-biasing of the back gates, the IG FinFETs in I3 are made weaker compared to the drive inverter (I1). As a result, the drive inverter need not be oversized, as conventionally done, ensuring a safe write operation at the same time. At nominal process corners, the IG latch leads to 33% less leakage power and 20% less area compared to the conventional SG latch with almost no degradation in propagation delay and setup time. Similar power and area improvements are obtained for IG flip-flops relative to TG flip-flops (Figure 24(a)). Bhoj and Jha introduced ASG FinFETs in the TG and HS latches and observed similar tradeoffs. Introducing ASG FinFETs in all the latch inverters (I1, I2, and I3) results in a minimum-leakage and maximum-delay configuration. Introducing ASG FinFETs in only I3 leads to a configuration similar to the IG latch. The new configuration reduces leakage power by approximately 50%,

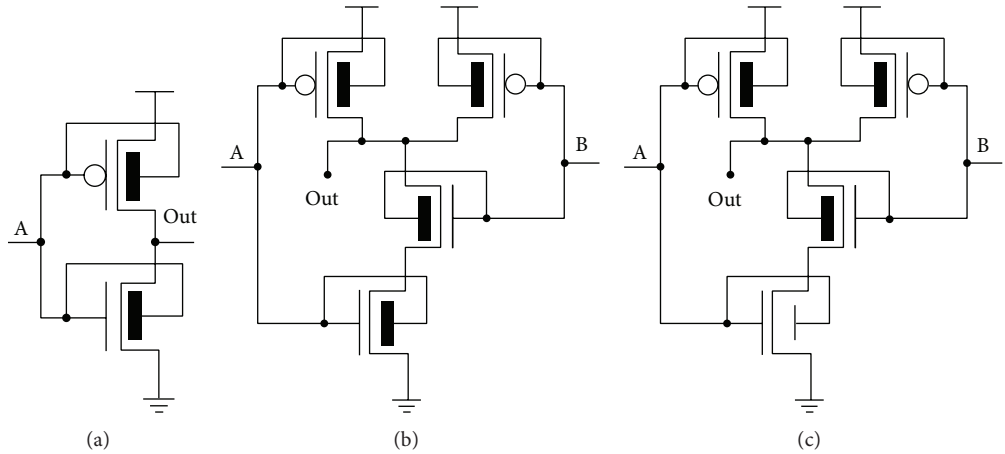

Figure 21: Schematic diagrams of ASG FinFET logic gates: (a) INV, (b) NAND2, and (c) NAND2S [49].

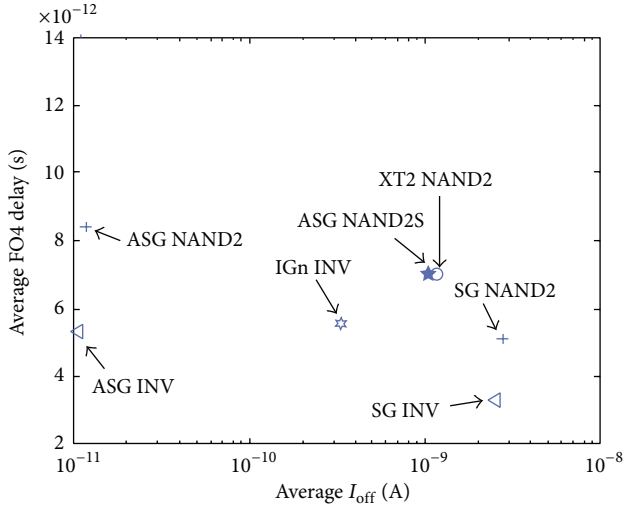

Figure 22: The leakage-delay spectrum of various logic gates [49].

but the propagation delay increases by roughly 30%. This configuration also results in area savings as I1 can be sized down, maintaining the desired write stability. Similar results are obtained for ASG flip-flops as well.

As in the case of TG latches and flip-flops, combinations of SG, IG, and ASG FinFETs in inverters (I1 and I2) and nFinFETs (N1 to N4) generate various HS latches (Figure 23(b)) and flip-flops (Figure 24(b)). As expected, the leakage power of the all-ASG configuration is reduced by almost 65%, however, at the expense of doubling of its propagation delay. Using ASG FinFETs in N2/N4 only makes an interesting configuration that results in around 20% improvement in leakage, but only at a negligible cost (less than 5%) in propagation delay. Similar results were obtained for HS flip-flops.

4.5. SRAM. SRAM is a key component of on-chip caches of state-of-the-art microprocessors. In today's multicore processors, typically more than half of the die area is dedicated to SRAMs [106]. Since SRAMs are built with the smallest transistors possible at a technology node (in order to increase the memory density), statistical fluctuations are extremely detrimental to SRAM performance. Deeply scaled SRAMs, built atop planar MOSFETs, suffer from mismatches in transistor strengths and V_{th} caused by RDF and other sources of process variations. SRAMs also consume most of the chip's total leakage power because of very long idle periods in large memory arrays. Six-transistor (6T) FinFET SRAMs (as shown in Figure 25) have been explored quite thoroughly in the past decade from the point of view of suppressing leakage power and tackling increased variability among bitcells [52–60, 64, 65]. Figure 26 shows the butterfly curves, under process variations, for MOSFET and FinFET based SRAMs. The curves clearly demonstrate that FinFET SRAMs have a superior static noise margin (SNM) because they do not suffer from RDF.

New SRAM bitcell structures have been proposed using a mix of SG, IG, and ASG FinFETs [55, 56, 60, 62]. In [55], FinFET SRAMs have been classified into the following categories: (i) vanilla shorted-gate configurations (VSCs) in which all FinFETs are SG, (ii) independent-gate configurations (IGCs) in which one or more SG FinFETs are replaced with IG FinFETs, and (iii) multiple workfunction shorted-gate configurations (MSCs) in which one or more SG FinFETs are replaced with ASG FinFETs. Table 4 shows the best bitcells from the perspectives of different metrics. RPNM, WTP, I_{READ}, I_{off}, T_R, and T_W refer to the read power noise margin, write-trip power, read current, leakage current, read access time, and write access time of the bitcell, respectively. Out of these, T_R and T_W represent transient metrics whereas the remaining metrics are DC. In Table 4, V (*mnp*) and A (*mnp*) refer to VSC and MSC bitcells that have *m*, *n*, and *p* fins in the pull-up (PU), pass-gate (PG), and pull-down (PD) FinFETs, respectively. Pass-gate feedback (PGFB) [59], pull-up write gating (PUWG) [60], split pull-up (SPU) [65], and row-based back-gate bias (RBB) [64] are some popular IGC FinFET SRAM bitcells, as shown in Figure 27. Table 4 also indicates that there is no single SRAM cell that is the best in all the metrics, but it is possible to find a cell that is ahead of

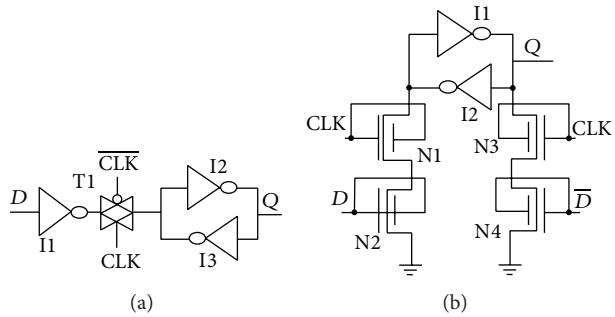

Figure 23: Schematic diagrams of FinFET latches: (a) transmission-gate and (b) half-swing [49].

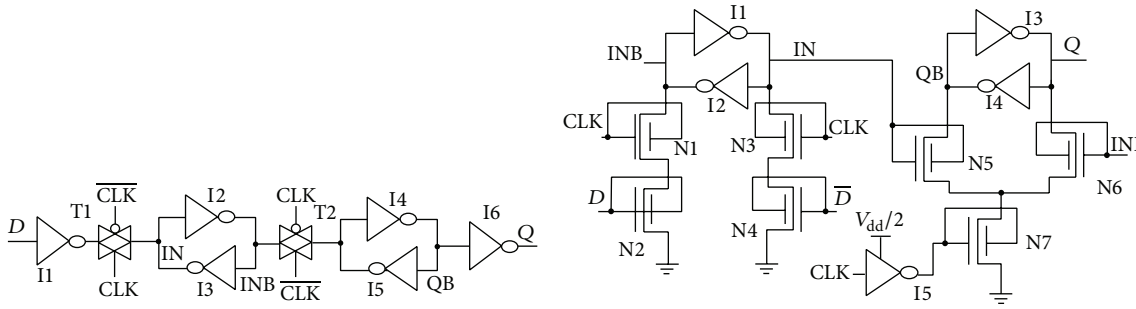

Figure 24: Schematic diagrams of FinFET flip-flops: (a) transmission-gate and (b) half-swing [49].

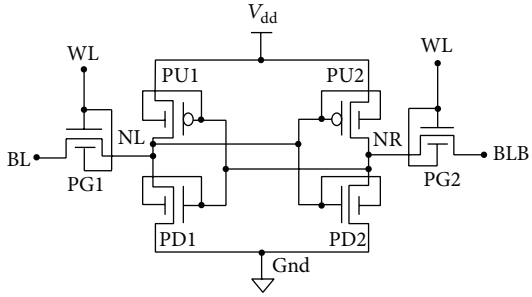

Figure 25: Schematic diagram of a 6T FinFET SRAM.

Table 4: Comparison of FinFET SRAM cells [55].

Metric	VSC	IGC	MSC
Max. RPNM	V(113)	PGFB-PUWG	A(112)
Min. WTP	V(122)	PGFB-SPU	A(111)
Max. I_{READ}	V(135)	RBB	A(112)
Min. I_{off}	V(111)	RBB	DPG-H
Min. T_R	V(111)	PGFB	A(11)S
Min. T_W	V(111)	PGFB-SPU	A(111)

the others in some of the metrics. A careful look at the absolute values of the metrics reveals that IGC bitcells exhibit superior DC metric values relative to those of VSC bitcells, but their poor transient performance makes them unattractive. On the other hand, MSC bitcells have competitive DC metric values and better transient performance relative to VSC bitcells. Hence, in a nutshell, MSC bitcells may be a good choice for a FinFET SRAM bitcell. Out of all MSC bitcells, A(111) seems to be the most promising one. It is also shown in [55] that the transient behavior of a bitcell is very important to account for. Evaluations based on only DC metrics may lead to incorrect conclusions.

Goel et al. proposed a different FinFET SRAM bitcell using ADSE FinFETs in the access transistors (i.e., the PG FinFETs) [57]. When the extended spacers of the PG FinFETs are placed towards the internal storage nodes (NL and NR) of the bitcell, it is called contact-underlap-storage (CUS) SRAM. This SRAM exploits the bidirectional current flow in ADSE FinFETs to improve both the read and write margins (by 11% and 6%, resp.). Also, it reduces the leakage current by as much as 57%. However, it suffers from a degraded access time (7%) and cell area (7%).

Moradi et al. proposed a FinFET SRAM bitcell that exploits AD FinFETs [58]. The lowly doped drains of the AD-access transistors are placed towards the storage nodes. This SRAM bitcell is able to resolve the read-write conflicts as the strength of the access transistors varies based on the voltage of the storage nodes. This boosts both read (7.3%) and write (23%) margins. These improvements come at the cost of an increased access time (42%) because the access transistor becomes weak during a read operation. Improvement in subthreshold leakage of this bitcell is also to be noted (2.8×).

Sachid and Hu showed that multiple fin-height FinFETs can be used to design more dense and stable SRAMs [61].

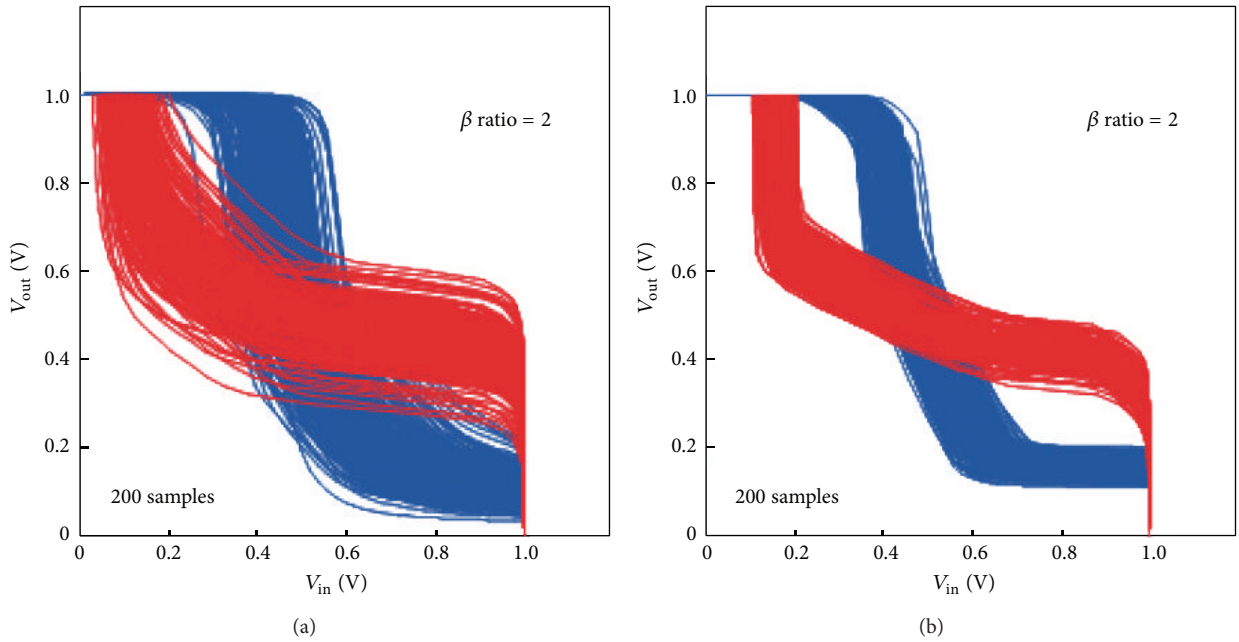

FIGURE 26: Butterfly curves for SRAMs implemented with 20 nm gate-length (a) bulk planar MOSFET and (b) FinFET. The FinFET SRAM exhibits a superior SNM because of smaller V_{th} variation due to the use of an undoped channel [95].

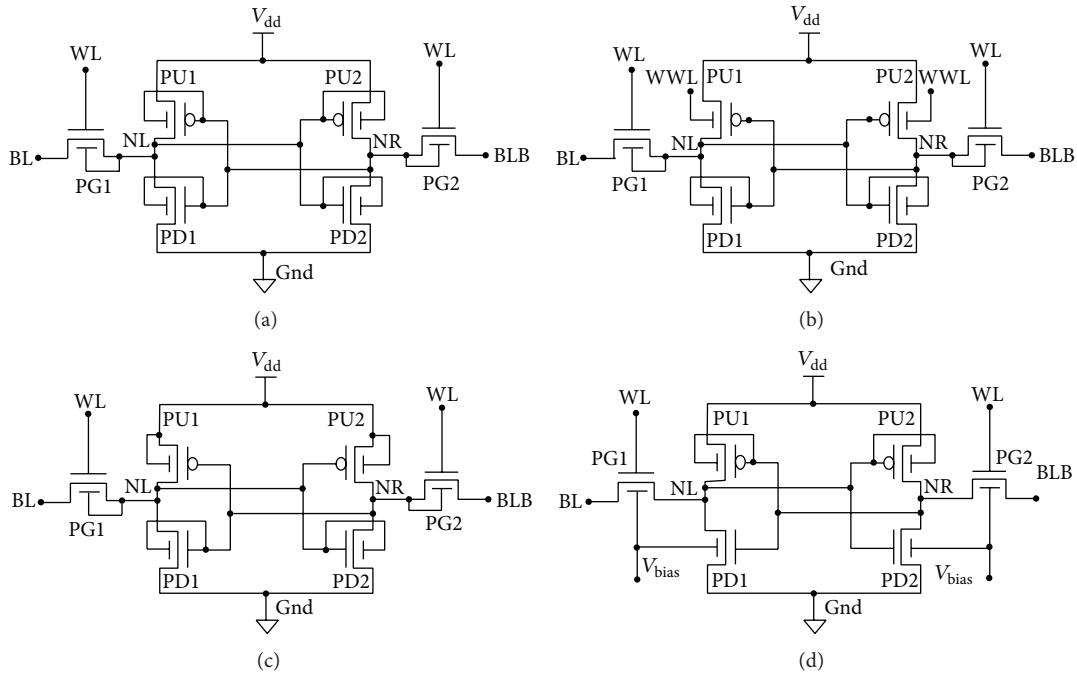

FIGURE 27: Schematic diagrams of FinFET SRAM bitcells: (a) PGFB, (b) PGFB-PUWG, (c) PGFB-SPU, and (d) RBB.

Using multiple fin heights enables better control over the strengths of PU, PG, and PD transistors, leading to a better noise margin, without incurring any area penalty. The drawbacks of this scheme are increased leakage power and process complexity.

4.6. DRAM. One-transistor dynamic random-access memories (1T-DRAMs) have traditionally been used both in off-chip main memory and on-chip caches due to their significant area advantage over SRAMs. With the advent of partially depleted-SOI (PDSOI) technology, a capacitorless 1T-DRAM, also known as floating-body cell (FBC), was proposed. This DRAM leads to a smaller area and a less complicated fabrication process than conventional embedded DRAMs [107–109]. Its functionality is based on the V_{th} shift produced by majority carrier accumulation in the floating

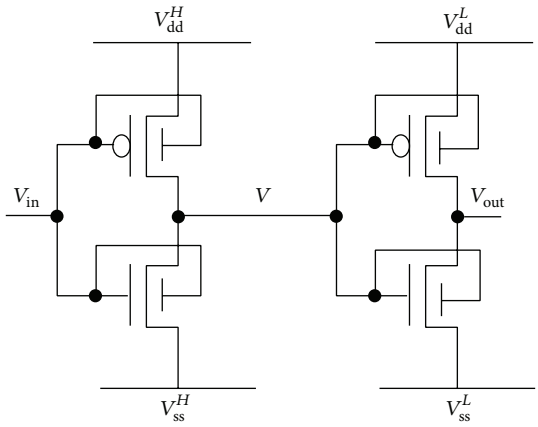

Figure 28: Buffer design using TCMS [34].

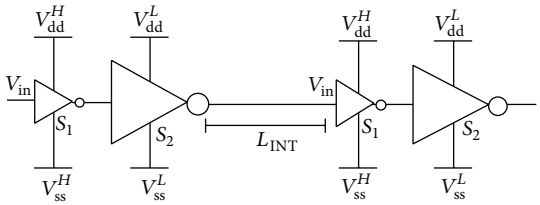

Figure 29: Interconnect design using TCMS [34].

body. However, the higher impurity concentration required to suppress SCEs degrades the retention characteristics of planar PDSOI 1T-DRAMs. Double-gate FinFET DRAMs (DG FinDRAM) are able to overcome these scaling issues of 1T-DRAMs [110–112]. The second gate, with the application of an appropriate bias, helps with the accumulation of majority carriers and thereby relaxes the high impurity concentration criterion. FinFET based 1T-DRAMs also exhibit long retention times and large sense margins. Thus, they have emerged as a promising embedded memory alternative.

5. Circuit-Level Analysis

Logic circuit analysis and optimization tools have been implemented using FinFET based standard cell libraries described in the previous section. In this section, we describe them in brief.

5.1. Analysis. FinPrin is a statistical static timing analysis (SSTA) and power analysis tool for FinFET logic circuits that considers PVT variations and is based on accurate statistical models for delay, dynamic power, and leakage power of the logic netlist [113]. It takes a register transfer-level (RTL) or gate-level description of a netlist as an input and estimates leakage/dynamic power and delay distributions (μ and σ for Gaussian distributions) at every node of the netlist, based on the circuit-level parameter values provided in the FinFET design library, such as input and output capacitance, input and output resistance, and leakage current, taking into account the impact of PVT variations. The leakage and temperature variation models are macromodel based [94], whereas the delay models are based on an SSTA approach [114]. These models also take spatial correlations of the gates into account using a rectangular grid based method [115]. FinPrin's performance has been compared with that of accurate quasi-Monte Carlo (QMC) simulations [116, 117] and was shown to produce very accurate means (μ) and reasonably accurate standard deviations (σ), while enabling a significant computation time speedup (two orders of magnitude).

5.2. Optimization. Optimization of logic circuits is made possible by accurate analysis. Synopsys Design Compiler is commercially used for power/delay optimization of logic circuits, given a standard cell library [99]. In order to exploit the various FinFET design styles, a linear programming based optimization algorithm and tool are proposed in [39]. The algorithm is used to assign gate sizes and FinFET types to the mapped circuit, under a timing constraint, by selecting standard cells from the FinFET design library. Unlike traditional greedy gate-sizing algorithms, this algorithm divides the available slack among gates whose cells may be replaced. It is shown that this approach can achieve 15–30% better power consumption than Synopsys Design Compiler [39].

5.3. Novel Interconnect Structures and Logic Synthesis. Interconnects assume a lot of importance in deeply scaled technology nodes as they govern the delay and power consumption of modern integrated circuits. FinFETs not only provide newer circuit design styles, but also can lead to an efficient interconnect implementation strategy. A mechanism to improve the interconnect efficiency, called threshold voltage control through multiple supply voltages (TCMS), has been proposed in [34]. The TCMS principle is based on the fact that the back-gate bias of a FinFET affects the V_{th} of the front gate. Instead of using the conventional dual-V_{dd} scheme, TCMS uses a slightly higher supply voltage (V_{dd}^H) and a slightly negative supply voltage (V_{ss}^H) along with the nominal supply voltages, V_{dd}^L, and ground (which is referred to as V_{ss}^L for symmetry). TCMS is based on the observation that an overdriven inverter (i.e., whose input is driven by an inverter supplied with V_{dd}^H and V_{ss}^H and whose supply voltage is V_{dd}^L), as shown in Figure 28, has both less leakage and less delay. Less leakage is ensured because of an increase in the V_{th} of the leaking transistor and less delay is ensured because of the higher current drive in the active transistor. The improvement in the drive strength of the active transistor results in improved delay that can be traded off for area and power reduction under a given timing constraint. A chain of such inverter pairs can be formed on the interconnect, as shown in Figure 29, without the need for voltage-level shifters due to the use of higher-V_{th} transistors in the inverter supplied with V_{dd}^H and V_{ss}^H. This scheme enables a significant reduction in subthreshold leakage power in TCMS buffer interconnects. It has been shown that, on an average, TCMS provides overall power savings of 50.4% along with area savings of 9.2% as compared to a state-of-the-art dual-V_{dd} interconnect synthesis scheme [34].

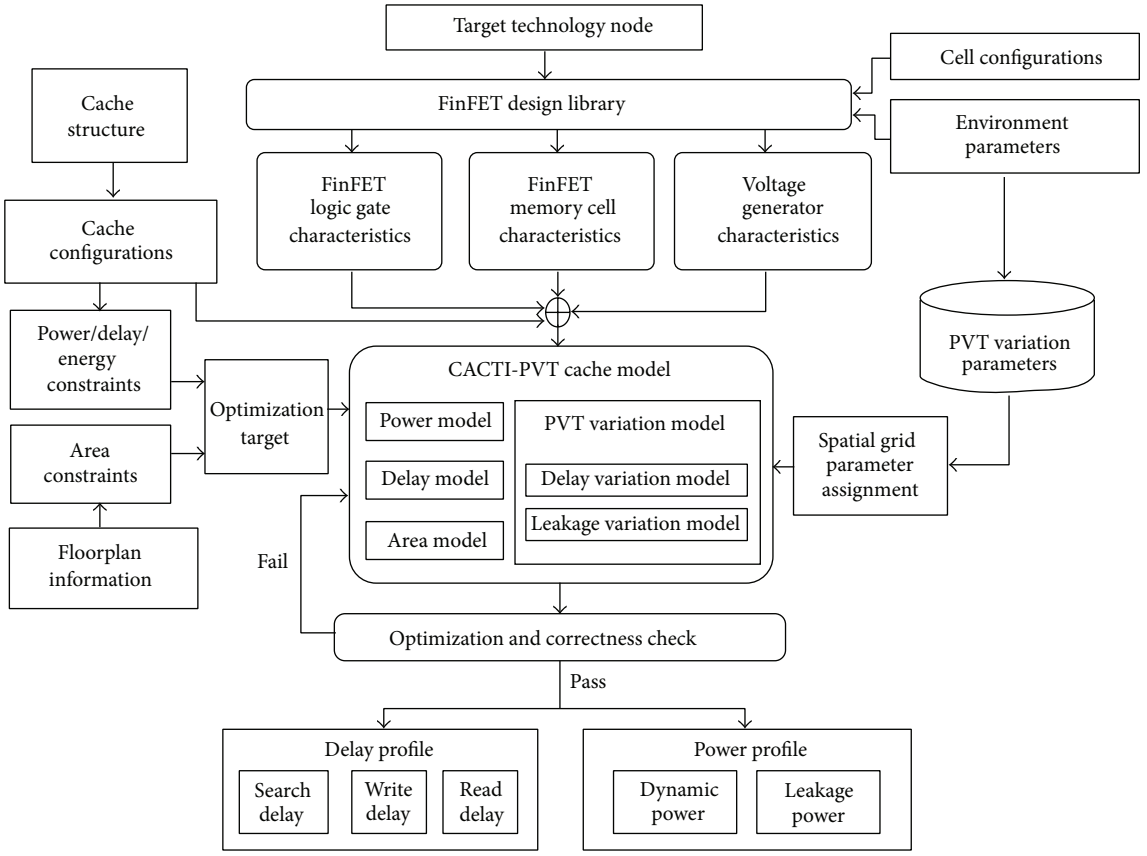

Figure 30: CACTI-PVT block diagram [69].

The TCMS principle can also be applied to logic synthesis [35]. In this case, a FinFET logic gate can take advantage of the TCMS principle if its input arrives from a gate supplied with the V_{dd}^{H} set and its supply voltage belongs to the V_{dd}^{L} set. Since the opposite scenario leads to a high leakage current, it is avoided. Based on the combinations of supply voltage (V_{dd}^{L} or V_{dd}^{H}), input voltage (V_{dd}^{L} or V_{dd}^{H}), and threshold voltage (high-V_{th} or low-V_{th}), INV and NAND2 have seven and 25 variants, respectively. As in the case of the interconnects, use of high-V_{th} FinFETs in V_{dd}^{H} gates that need to be driven by a V_{dd}^{L} input voltage obviates the need for a voltage-level converter between the V_{dd}^{L} and V_{dd}^{H} gates. With the use of a linear programming based optimization algorithm, TCMS leads to an overall power reduction of 3× under relaxed delay constraints.

6. Architecture-Level Analysis

Next, we ascend the design hierarchy to the architecture level. Due to shrinking feature sizes and severe process variations, the delay and power consumption at the chip level are not easy to predict any more [114]. Because of their inherent statistical nature, a yield analysis of an integrated circuit (under a design constraint) has become very important. This analysis estimates the percentage of chips that will meet the given power and delay constraints for the particular chip architecture for a given process. In the following subsections, we discuss PVT-aware simulation tools for various FinFET based architectural components.

6.1. FinFET Based Caches. An integrated PVT variation-aware power-delay simulation framework, called FinCANON [69], has been developed for FinFET based caches and NoCs. It has two components: CACTI-PVT for caches and ORION-PVT for NoCs. CACTI-PVT is an extension of CACT-FinFET [67]. CACTI-PVT can be used to obtain the delay and leakage distributions of FinFET based caches with varying sizes, SRAM cell types, and back-gate biases. The block diagram of CACTI-PVT is shown in Figure 30. It uses a FinFET design library consisting of FinFET logic gates of various sizes and types and different types of FinFET SRAM cells. This library is characterized using accurate device simulation. The process variation models used in CACTI-PVT are calibrated using QMC simulations, along with the rectangular grid-based method to model spatial correlations. Peripheral components implemented with SG FinFETs and SRAM cells implemented with some IG FinFETs or ASG FinFETs provide the best balance between delay and leakage of the FinFET caches.

6.2. FinFET Based NoCs. With increasing number of cores in chip multiprocessors (CMPs), NoCs have emerged as an

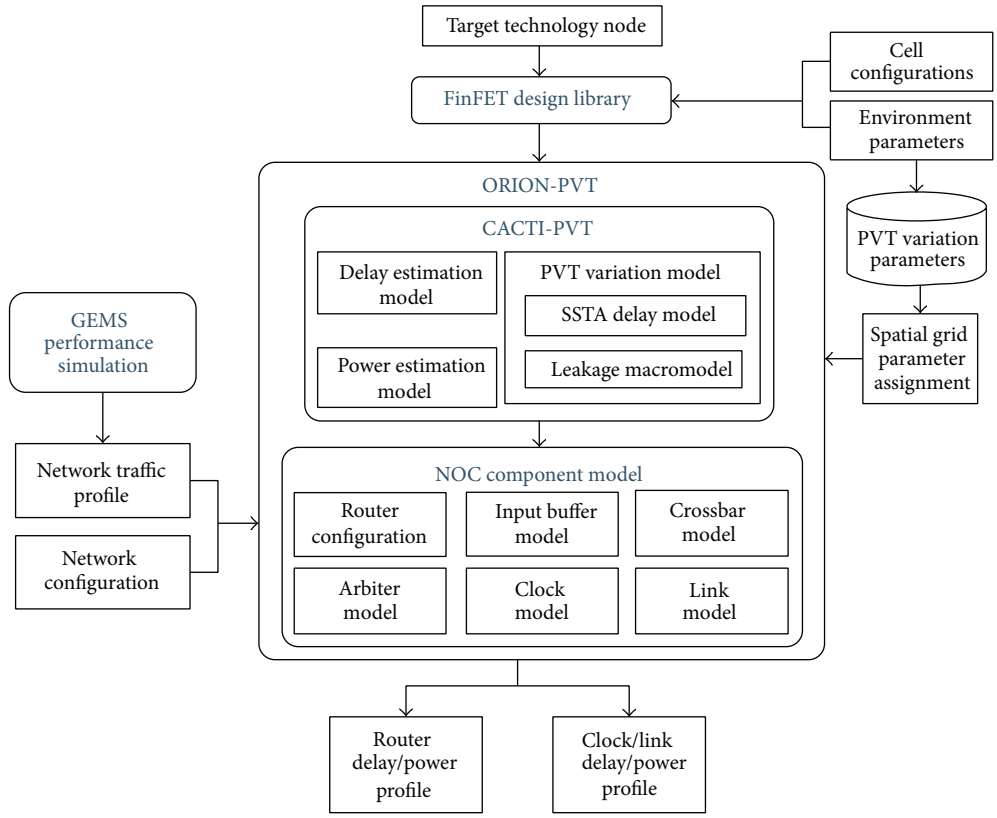

Figure 31: ORION-PVT block diagram [69].

effective communication mechanism among the cores. FinCANON also includes a performance/power simulation tool, called ORION-PVT, aimed at FinFET NoCs [69]. ORION-PVT, whose block diagram is shown in Figure 31, is an extension of ORION-FinFET [68]. Here, an SSTA technique and a macromodel based methodology are used to model the PVT variations in delay and leakage. It also provides a power breakdown of an on-chip router. Leakage power is found to dominate the total power of the router at higher temperatures.

A FinFET based implementation of a variable-pipeline-stage router (VPSR) is proposed in [70]. VPSR enables dynamic adjustment of the number of pipeline stages in the router based on incoming network traffic. As a result, different flow control digits (flits) may traverse pipeline stages of varying lengths while passing through the router. This leads to enhanced router performance because VPSR adapts its throughput to the network traffic requirement at runtime. VPSR also enables significant savings in leakage power through reverse-biasing (called adaptive back-gate biasing) of the back gates of IG FinFETs in infrequently accessed components of the router.

6.3. FinFET Based Multicore Processors. In the computer architecture domain, the trend has shifted in recent years from uniprocessors to CMPs and multicore systems in order to serve the ever-increasing performance demand. Tools like FinCANON have paved the way for a more powerful tool for characterizing multicore processors. McPAT-PVT is a PVT variation-aware integrated power-delay simulation tool for FinFET based multicore processors [71]. Figure 32 shows the block diagram of McPAT-PVT. It has two key components: processor model and yield analyzer. The processor model contains power/delay macromodels of various functional units (e.g., arithmetic-logic unit, floating-point unit, memory management unit, etc.) of the processor core. The yield analyzer can predict the yield of a specified processor configuration under PVT variations. Figure 33 zooms into the components of the processor model. The efficacy of this tool has been demonstrated on an alpha-like processor core and multicore simulations based on Princeton Application Repository for Shared-Memory Computer (PARSEC) benchmarks.

7. Conclusion

In this paper, we have explored the impact of FinFETs from the device to architecture level. We learnt about the shortcomings of planar MOSFETs in today's deeply scaled technologies and the advantages of FinFETs as suitable replacements for planar MOSFETs. We looked into FinFET device characteristics and evaluated tradeoffs among SG, IG, and ASG FinFETs, along with other FinFET asymmetries, such as drain-spacer extension, source/drain doping, gate-oxide thickness, and fin height. We learnt about the detrimental impact of PVT variations on FinFET chip performance

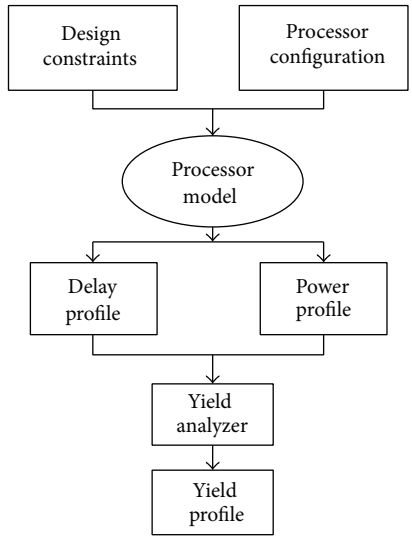

Figure 32: McPAT-PVT block diagram [71].

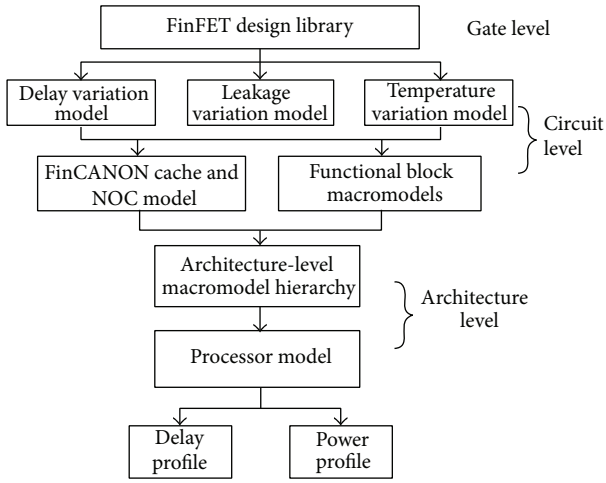

Figure 33: McPAT-PVT processor models [71].

and power. We surveyed techniques for characterizing FinFET devices and circuits and explored FinFET based logic gates, flip-flops, and memory cells. Finally, we also reviewed PVT variation-aware FinFET circuit- and architecture-level simulation tools. We observed leakage-delay tradeoffs that are possible at each level of the design hierarchy. The availability of a plethora of FinFET styles opens up new design opportunities at each level, which we hope some of the readers will be willing to explore.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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