

Research Article

Design of Low Power and Efficient Carry Select Adder Using 3-T XOR Gate

Gagandeep Singh and Chakshu Goel

ECE Department, Shaheed Bhagat Singh State Technical Campus, Ferozepur, Punjab 152004, India

Correspondence should be addressed to Chakshu Goel; chakshu77@yahoo.com

Received 16 June 2014; Accepted 7 September 2014; Published 22 September 2014

Academic Editor: Liwen Sang

Copyright © 2014 G. Singh and C. Goel. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

In digital systems, mostly adder lies in the critical path that affects the overall performance of the system. To perform fast addition operation at low cost, carry select adder (CSLA) is the most suitable among conventional adder structures. In this paper, a 3-T XOR gate is used to design an 8-bit CSLA as XOR gates are the essential blocks in designing higher bit adders. The proposed CSLA has reduced transistor count and has lesser power consumption as well as power-delay product (PDP) as compared to regular CSLA and modified CSLA.

1. Introduction

In today's VLSI circuit designs, there is a significant increase in the power consumption due to the increasing speed and complexity of the circuits. As the demand for portable equipment like laptops and cellular phones is increasing rapidly, great attention has been focused on power efficient circuit designs [1–4]. Adders are the basic building blocks of the complex arithmetic circuits. Adders are widely used in Central Processing Unit (CPU), Arithmetic Logic Unit (ALU), and floating point units, for address generation in case of cache or memory access and in digital signal processing [5–7].

Having adders with fast addition operation and low power along with low area consumption is still a challenging issue. Depending upon the area, delay, and power consumption, the various adders are categorized as ripple carry adder (RCA), carry select adder (CSLA), and carry lookahead adder (CLAA). CSLA provides a compromise between the large area with small delay of CLAA and small area but longer delay of RCA [8]. CSLA uses pair of RCAs for addition, that is, one block of RCA with $C_{in}(\text{carry in}) = 0$ and other block of RCA with $C_{in} = 1$. Depending on the value of previous carry, the final sum and carry outputs are selected using multiplexer. Due to the pair of RCAs used for each bit addition, the simplest kind of CSLA is not very efficient [9].

Keeping in mind that XOR gates are the building blocks of adders, here in this work, we use a 3T-XOR gate to design an 8-bit CSLA. The main advantage of using 3T-XOR gate is that the power consumption of the circuit decreases due to the large decrease in number of switching transistors (MOSFETs) used in the design of 8-bit CSLA.

This paper is organized as follows. Section 2 presents the earlier works on carry select adder including the detailed structure of regular CSLA as well as modified CSLA. Section 3 explains the proposed CSLA and evaluates the reduction in switching transistors (MOSFETs) count. The implementation details as well as simulation results of proposed CSLA are analyzed in Section 4 and Section 5 concludes the whole work.

2. Earlier Works on Carry Select Adder

In digital adders, the speed of addition is limited due to the time taken by the carry signal to propagate through the adder. The regular carry select adder (R-CSLA) was introduced to mitigate the problem of carry propagation delay by independently generating multiple carries and then selecting the correct sum and carry outputs depending on the value of previous carry [9]. As previously discussed, this type of CSLA (i.e., R-CSLA) was not area efficient due to the use of pair of RCAs (each for $C_{in} = 0$ and $C_{in} = 1$) to produce

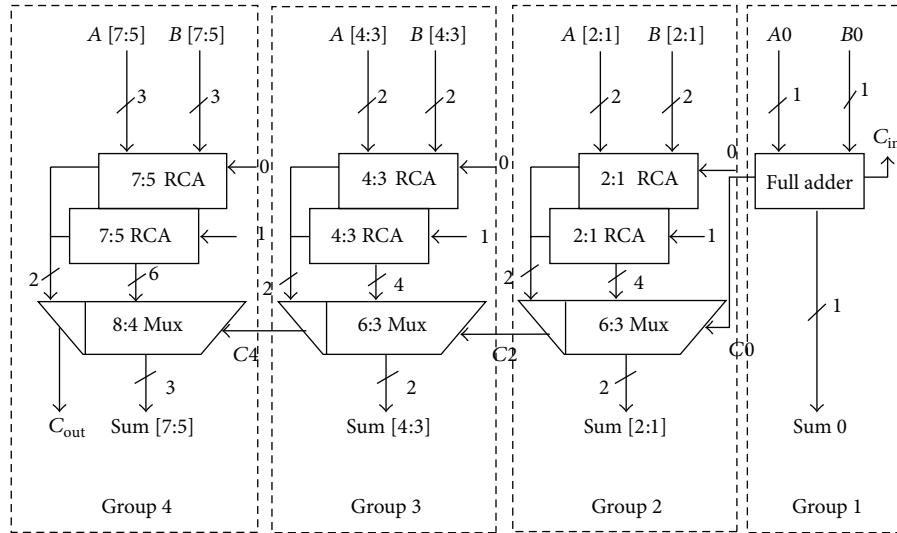


FIGURE 1: Regular 8-bit CSLA.

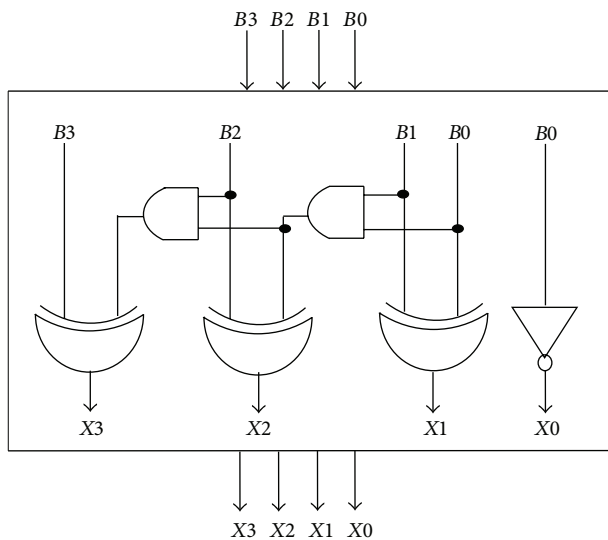


FIGURE 2: Four-bit BEC circuit.

TABLE 1: Truth table of 4-bit BEC.

$I [3:0]$	$X [3:0]$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

the final sum and carry output. The 8-bit R-CSLA is shown in Figure 1.

To make low power consumption and an area efficient CSLA, an add-one circuit known as Binary to Excess-1 Converter (BEC) circuit was introduced. This BEC circuit replaced the RCA with $C_{in} = 1$ used in R-CSLA as lesser numbers of logic gates were used in BEC as compared to n -bit RCA [10–12]. The truth table and circuit diagram of 4-bit BEC are shown in Figure 2 and Table 1, respectively.

The 8-bit modified carry select adder (M-CSLA) using BEC is shown in Figure 3. As shown in the Figure 3, 8-bit M-CSLA was divided into four groups with different bit sizes of RCA and BEC. M-CSLA consists of RCAs (for $C_{in} = 0$), BEC circuits (for $C_{in} = 1$), and multiplexers (MUX). One input to the MUX is sum along with carry outputs from RCA and another input to the MUX is sum along with carry outputs

from BEC circuit. The final sum and carry outputs are selected depending upon the value of previous carry which is inputted as the select line to the MUX [10].

3. Proposed Work on CSLA

In this work, we use a modified XOR gate as it forms the basic building block of CSLA. Here, we use a 3-T XOR gate instead of 12-T XOR gate used in previous designs of R-CSLA and M-CSLA which helps in more efficient design of 8-bit CSLA [13]. The circuit diagrams of 3-T XOR gate and proposed 8-bit CSLA are shown in Figures 4 and 5, respectively.

The overall performance of CSLA in terms of power consumption, transistor count, and power-delay product (PDP) can be enhanced by modifying the XOR gate. A single

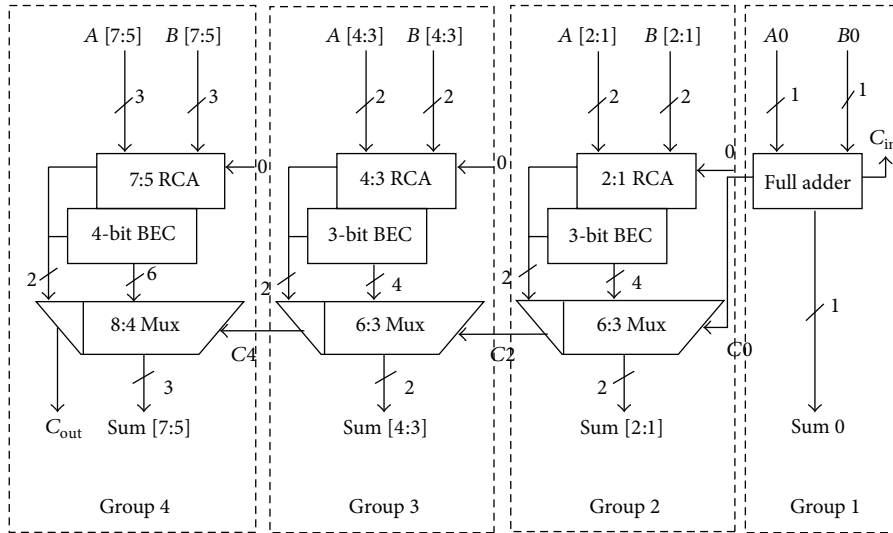


FIGURE 3: Modified 8-bit CSLA.

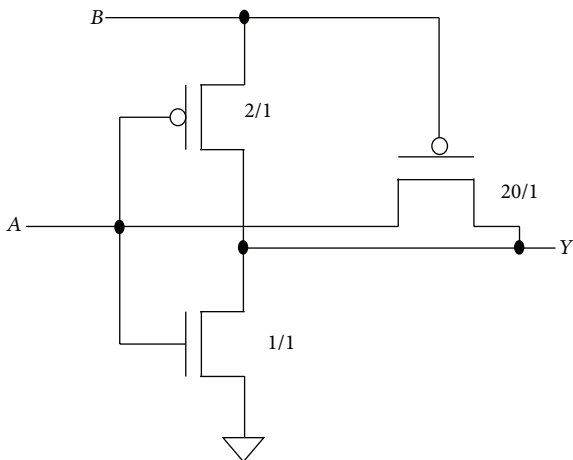


FIGURE 4: Three-T XOR gate.

modified XOR gate (3-T XOR gate) used in this work has 9 lesser transistors as compared to the XOR gate (12-T XOR gate) used in earlier works on CSLA. The proposed 8-bit CSLA is divided into 4 groups as shown in Figure 5.

The total reduction in transistor count for each group is calculated below.

Group 1. It contains one full adder. Each full adder consists of two XOR gates. Therefore total transistor count reduction for group 1 is

$$\begin{aligned} \text{number of XOR gates used} &= 2; \\ \text{transistor count reduction} &= 18 (2 * 9). \end{aligned}$$

Group 2. It contains one full adder, one half adder, and one 3-bit Binary to Excess-1 Converter (BEC). The transistor count reduction for group 2 is as follows:

$$\begin{aligned} \text{number of XOR gates used} &= 5 (2 + 1 + 2); \\ \text{transistor count reduction} &= 45 (5 * 9). \end{aligned}$$

Group 3. It contains one full adder, one half adder, and one 3-bit Binary to Excess-1 Converter (BEC). The transistor count reduction for group 2 is as follows:

$$\begin{aligned} \text{number of XOR gates used} &= 5 (2 + 1 + 2); \\ \text{transistor count reduction} &= 45 (5 * 9). \end{aligned}$$

Group 4. It contains two full adders, one half adder, and one 4-bit BEC. The transistor count reduction for group 4 is as follows:

$$\begin{aligned} \text{number of XOR gates used} &= 8 \{(2 * 2) + 1 + 3\}; \\ \text{transistor count reduction} &= 72 (8 * 9). \end{aligned}$$

Therefore the overall reduction in number of switching transistors (MOSFERTs) in proposed 8-bit CSLA as compared to the previously designed 8-bit M-CSLA is 180. Hence, the reduction in number of switching transistors reduces the power consumption as well as the power-delay product (PDP) of 8-bit CSLA.

4. Simulation Results

The proposed 8-bit CSLA has been successfully tested and synthesized in Tanner Tools using 90 nm technology with a supply voltage of 1.0 V. The power consumption and delay time of proposed 8-bit CSLA are calculated for all input conditions and the worst case power consumption as well as delay time is noted down. The power consumption, delay time, and power-delay product (PDP) of proposed 8-bit CSLA are compared with 8-bit R-CSLA and M-CSLA. The results of proposed 8-bit CSLA are also compared with the 8-bit CSA proposed in recent studies [14, 15]. The comparison is shown in Table 2.

It is clear from Table 2 that power consumption of proposed 8-bit CSLA is reduced by 27.7% and 21.7% when compared with R-CSLA and M-CSLA, respectively. The power-delay product (PDP) shows a similar trend as PDP is

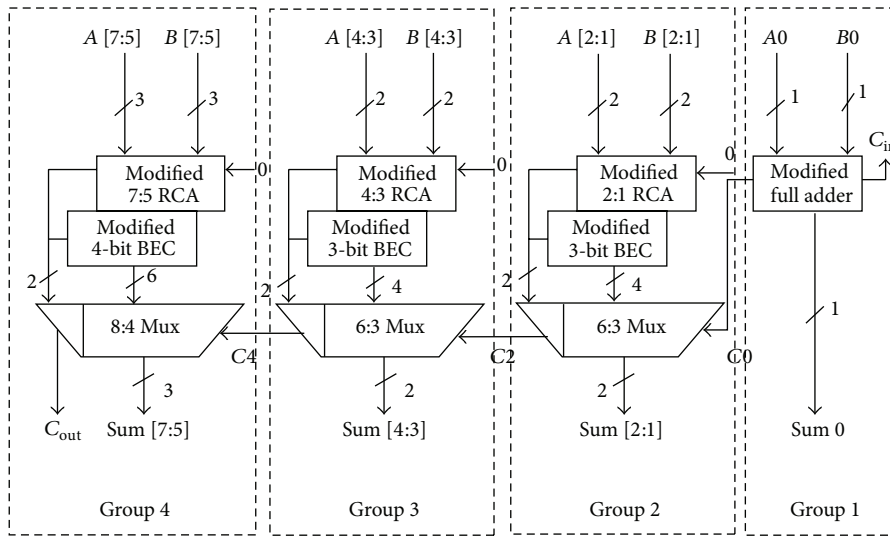


FIGURE 5: Proposed 8-bit CSLA.

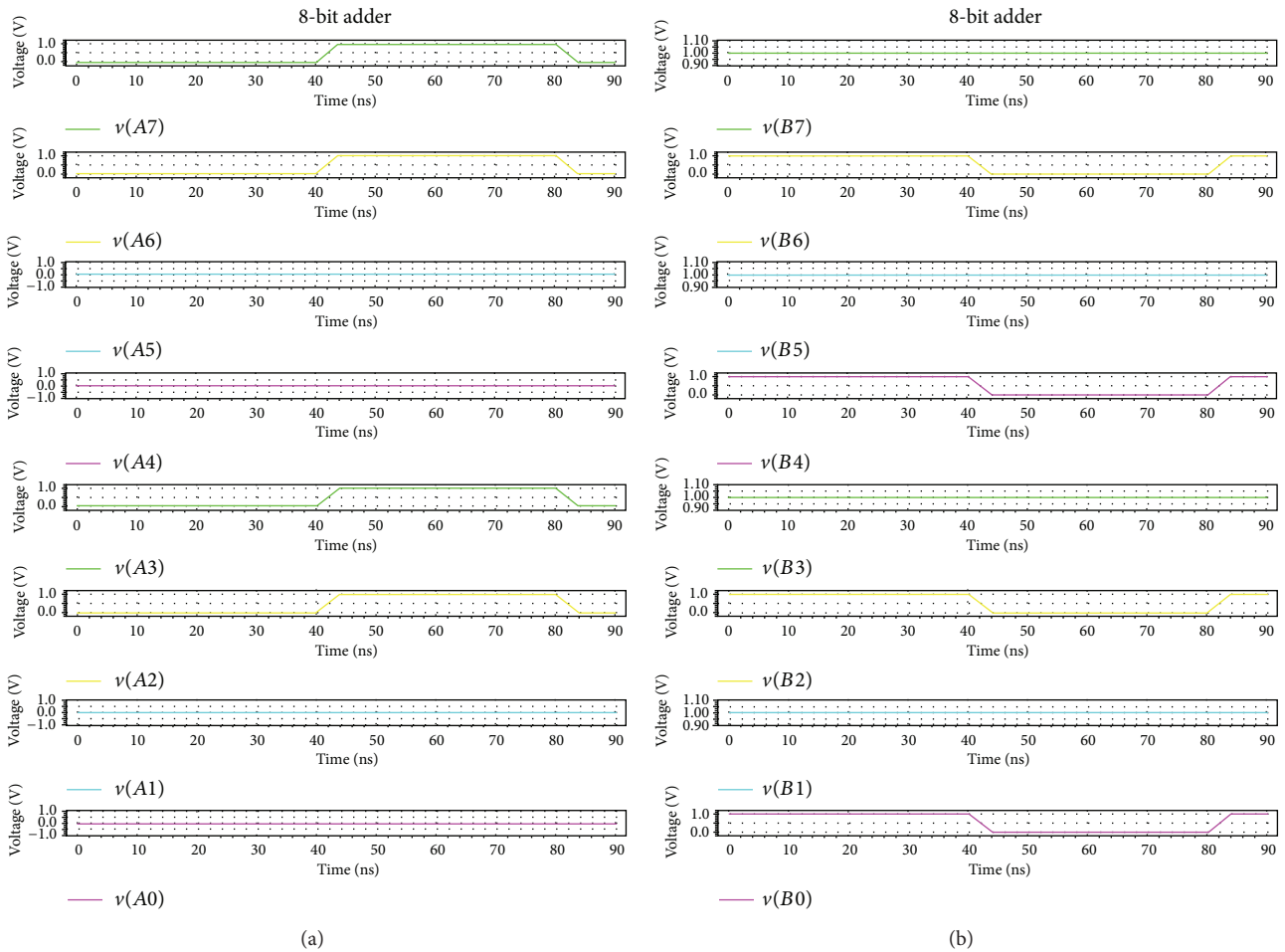


FIGURE 6: Postsimulation results: (a) input waveform A₀ to A₇ and (b) input waveform B₀ to B₇.

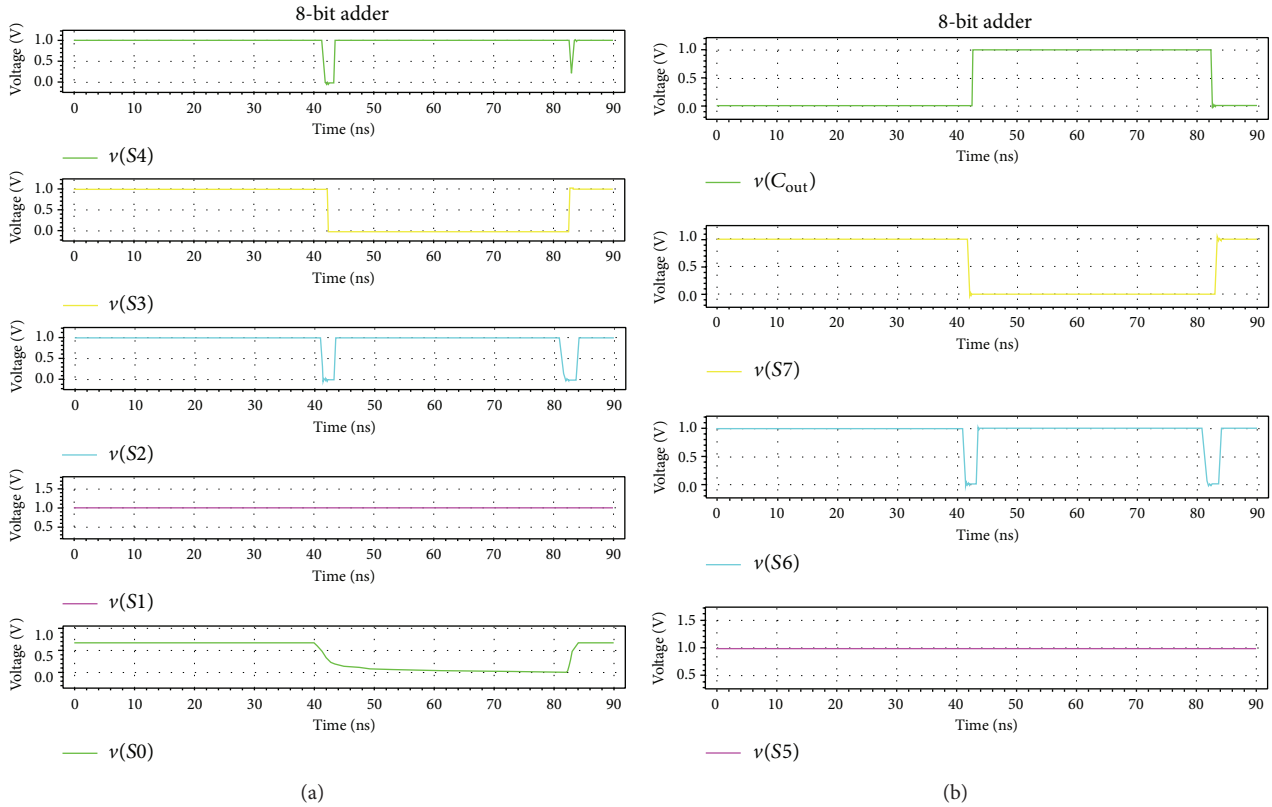


FIGURE 7: Postsimulation results: (a) output waveform S_0 to S_4 and (b) output waveform S_5 to S_7 and C_{out} .

TABLE 2: Comparison of various carry select adders.

Adder	Total power (μW)	Delay (ns)	Power-delay product (10^{-15})
8-bit regular CSLA	203.9	1.719	350.5
8-bit modified CSLA [10]	188.4	1.958	368.5
8-bit CSLA [14]	187.58	1.976	370.8
8-bit CSA using reversible logic [15]	180	17.2	3096
8-bit proposed CSLA	147.4	2.18	321.3

reduced by 8.3% and 12.8% when compared with R-CSLA and M-CSLA, respectively. Compared with the reversible logic style based 8-bit CSA [15], the proposed design has 18.1% reduction in power consumption and 89.6% reduction in PDP. Compared with the CSLA [14], the proposed CSLA has 21.7% reduction in power consumption and 13.3% reduction in PDP.

The postsimulation input-output waveforms for the 8-bit proposed CSLA are shown in Figures 6 and 7, respectively. The proposed design is simulated with a 12.5 MHz waveform with rise and fall times of 4 ns.

Figure 8 shows the comparison of various carry select adders in graphical form for the data given in Table 2. We can see from the graph that the proposed CSLA has minimum power-delay product (PDP) as well as the minimum power consumption when compared with regular CSLA, modified CSLA [10], CSLA [14], and reversible logic style based 8-bit CSA [15].

5. Conclusion

A simple approach of enhancing the performance of XOR gate to design an 8-bit CSLA is used in this paper. The proposed CSLA has large decrease in switching transistors (MOSFETs) due to the use of 3-T XOR gate. On comparing this proposed 8-bit CSLA with other existing 8-bit CSLAs like R-CSLA and M-CSLA, there is 27.7% and 21.7% reduction in power, respectively. The power-delay product (PDP) is also reduced by 8.3% and 12.8% when compared with R-CSLA and M-CSLA, respectively. The proposed 8-bit CSLA has the best performance compared with other 8-bit CSLAs present in literature. It would be interesting to design 16-bit CSLA and 32-bit CSLA using 3-T XOR gate.

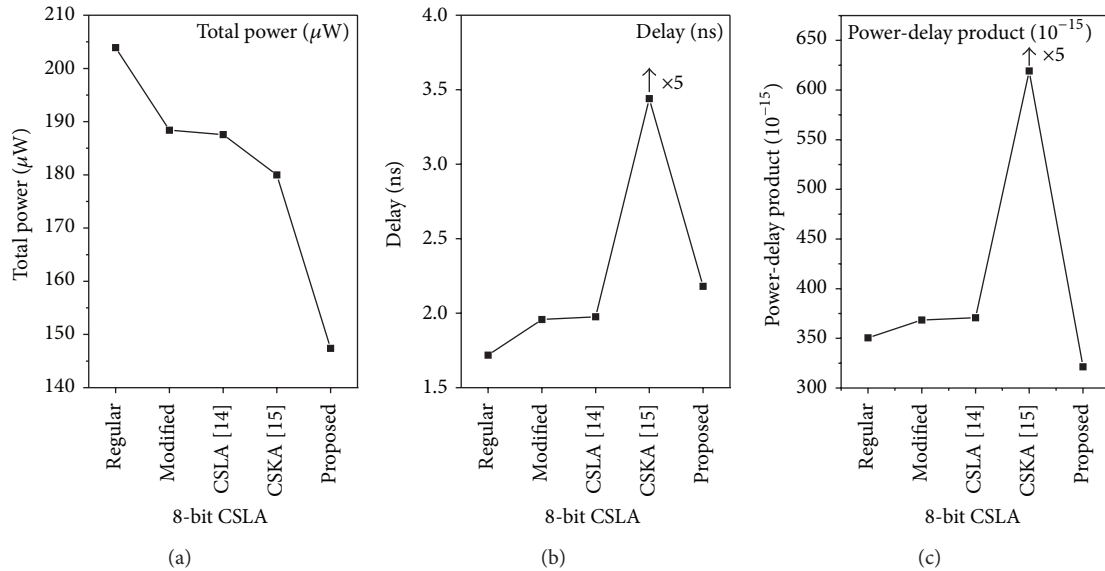


FIGURE 8: Power, delay, and PDP comparison of various CSLAs.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References

- [1] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low-power Full Adders based on majority-not gates," *Microelectronics Journal*, vol. 40, no. 1, pp. 126–130, 2009.
- [2] D. Wang, M. F. Yang, W. Cheng, X. G. Guan, Z. M. Zhu, and Y. T. Yang, "Novel low power full adder cells in 180 nm CMOS technology," in *Proceedings of the 4th IEEE Conference on Industrial Electronics and Applications (ICIEA '09)*, pp. 430–433, Xi'an, China, May 2009.
- [3] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*, Addison-Wesley, Reading, Mass, USA, 1993.
- [4] S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuit Analysis and Design*, McGraw-Hill, New York, NY, USA, 3rd edition, 2005.
- [5] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits, A Design Perspective*, Prentice Hall, Englewood Cliffs, NJ, USA, 2nd edition, 2002.
- [6] J. Uyemura, "CMOS Logic Circuit Design," Kluwer Academic Publishers, New York, NY, USA, 1999.
- [7] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*, Addison-Wesley, Reading, Mass, USA, 1993.
- [8] K. Rawat, T. Darwish, and M. Bayoumi, "A low power and reduced area carry select adder," in *Proceedings of the 45th Midwest Symposium on Circuits and Systems*, pp. I467–I470, August 2002.
- [9] O. J. Badrij, "Carry-select Adder," *IRE Transactions on Electronics Computers*, pp. 340–344, 1962.
- [10] B. Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 2, pp. 371–375, 2012.
- [11] T.-Y. Chang and M.-J. Hsiao, "Carry-select adder using single ripple-carry adder," *Electronics Letters*, vol. 34, no. 22, pp. 2101–2103, 1998.
- [12] Y. Kim and L. S. Kim, "64-bit carry-select adder with reduced area," *Electronics Letters*, vol. 37, no. 10, pp. 614–615, 2001.
- [13] S. R. Chowdhury, A. Banerjee, A. Roy, and H. Saha, "A high speed 8 transistor full adder design using novel 3 transistor XOR gates," *International Journal of Electronics, Circuits and Systems*, vol. 2, no. 4, pp. 217–223, 2008.
- [14] S. Singh and D. Kumar, "Design of area and power efficient modified carry select adder," *International Journal of Computer Applications*, vol. 33, no. 3, pp. 14–18, 2011.
- [15] S. Maity, B. Prasad De, and A. K. Singh, "Design and implementation of low-power high performance carry skip adder," *International Journal of Engineering and Advanced Technology*, vol. 1, no. 4, 2012.



Hindawi
Submit your manuscripts at
<http://www.hindawi.com>

