UNIT-3

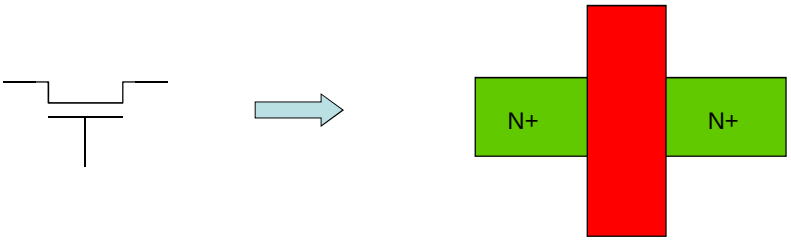
MOS AND BiCMOS Circuit Design Processes

MOS and BiCMOS Circuit Design Processes

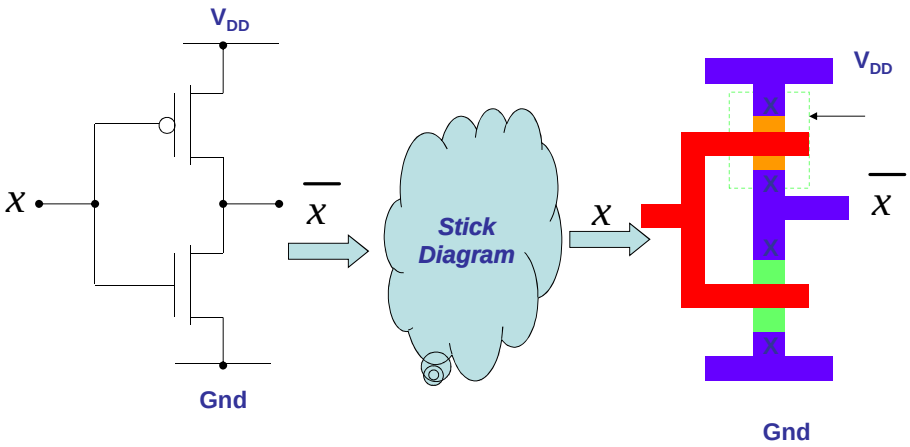
MOS layers

- Four basic layers….
  n-diffusion, P-diffusion,polysilicon,metal.
- The above layers are isolated from one another by thick or thin silicon dioxide insulating layers.
- **Thinox region-** n-diffusion/p-diffusion and channel area.
- To form contacts, layers are deliberately joined.
- The basic MOS transistor properties can be modified by additional implant in the thinox region**.**
- By addition of extra layers to CMOS process, BiCMOS devices can be fabricated

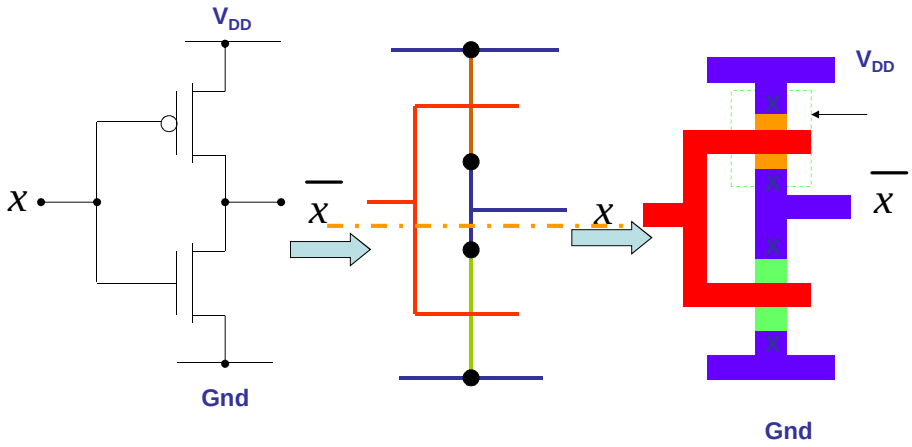
Stick diagrams



STICK DIAGRAMS



STICK DIAGRAMS



STICK DIAGRAMS

- VLSI design aims to translate circuit concepts onto silicon.
- stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through color codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.

Stick Diagrams

- Does show all components/vias.
- It shows relative placement of components.
- Goes one step closer to the layout
- Helps plan the layout and routing

A stick diagram is a cartoon of a layout.

Stick Diagrams

- Stick diagrams Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, well boundaries.
  - Any other low level details such as parasitics..

Stick Diagrams – Some rules

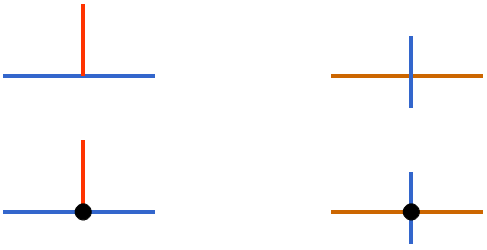
Rule 1.

When two or more ‘sticks’ of the same type cross or touch each other that represents electrical contact.

Stick Diagrams – Some rules

Rule 2.

When two or more ‘sticks’ of different type cross or touch each other there is no electrical contact. (If electrical contact is needed we have to show the connection explicitly).



Stick Diagrams – Some rules

Rule 3.

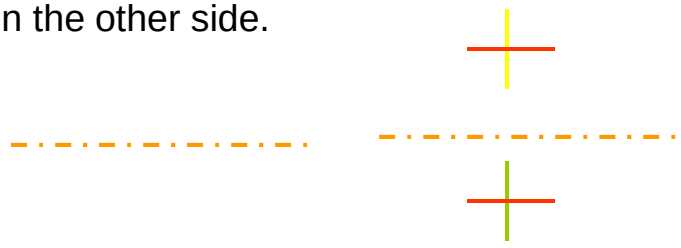
When a poly crosses diffusion it represents a transistor.

Note: If a contact is shown then it is ***not*** a transistor.

Stick Diagrams – Some rules

Rule 4.

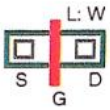
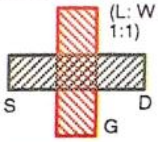
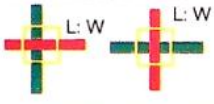
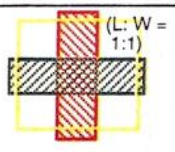
In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie on one side of the line and all nMOS will have to be on the other side.



Encodings for a simple single metal nMOS process

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n+ active) Thinox*	 *Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

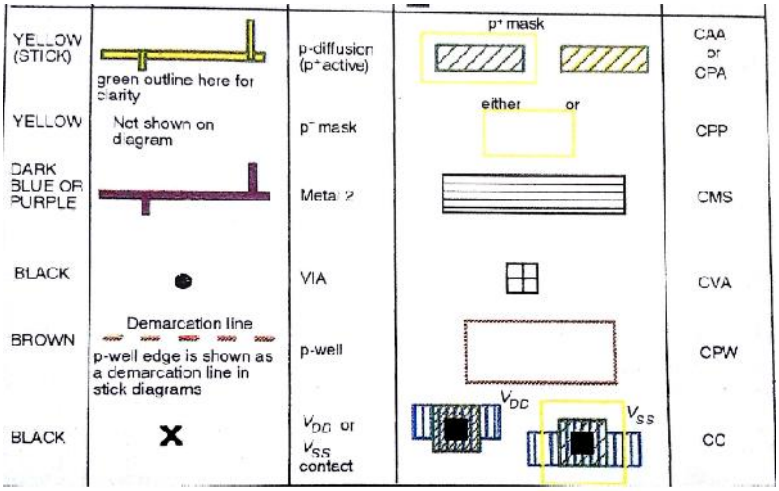
Encodings for a simple single metal nMOS process

FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor			
Transistor length to width ratio L: W should be shown.			
n-type depletion mode transistor nMOS only			
Source, drain and gate labelling will not normally be shown.			

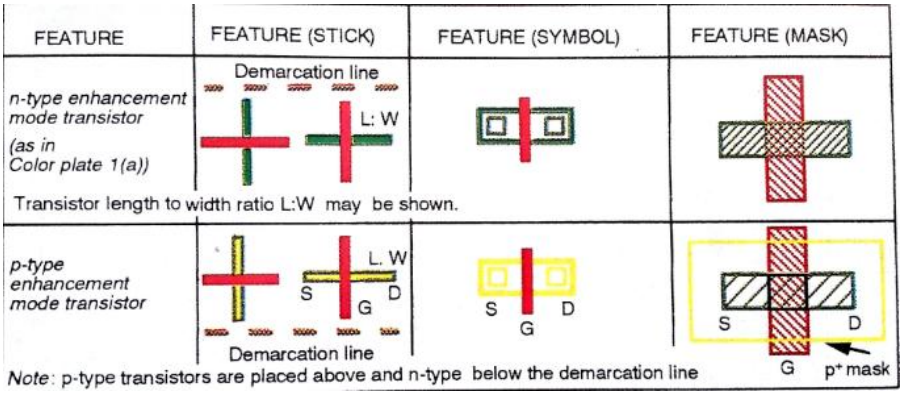
Color Encodings for a double metal CMOS p-well process.

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN	Encoding as in Color plate 1(a)	n-diffusion (n⁺ active) Thinox*	* Thinox = n-diff. + p-diff. + transistor channels	CAA or CNA
RED		Polysilicon	Encoding as in Color plate 1(a)	CPF
BLUE		Metal 1		CMF
BLACK		Contact cut		CC
GRAY		Overglass		COG

Color Encodings for a double metal CMOS p-well process.



Color Encodings for a double metal CMOS p-well process.



Design Rules and Layout

- The objective of design rules is to translate stick diagrams into actual geometry in silicon.
- Design rules are effective interface between circuit/system engineer and fabrication engineer.
- Layout is actual structure of any component (transistor,wires,contacts etc) implemented in silicon.
- Circuit engineers want tighter(small spacings between components),smaller layouts.
- Process engineers want design rules that result in controllable and reproducible process.

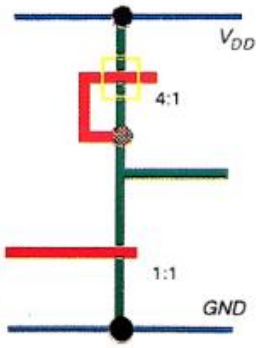
Why we need design rules

- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)
- Masks are tooling for manufacturing.
- Manufacturing processes have inherent limitations in accuracy.
- Design rules specify geometry of masks which will provide reasonable yields.
- Design rules are determined by experience.

Lambda Based Design Rules

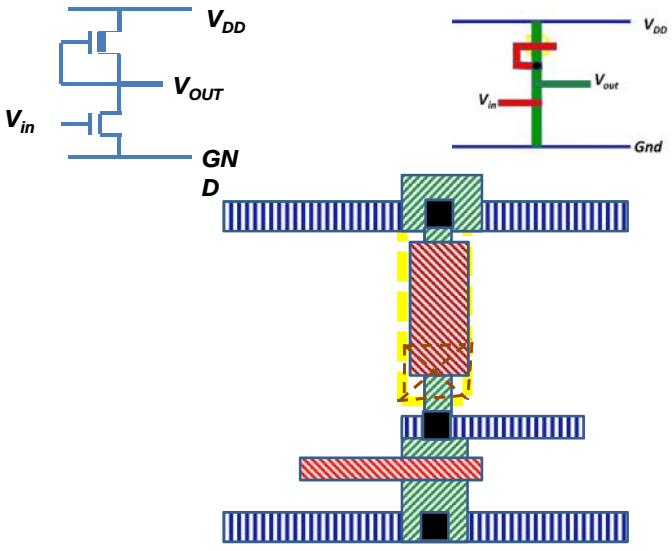
- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

Stick Diagram-nMOS inverter

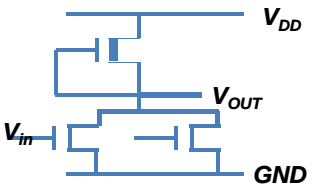


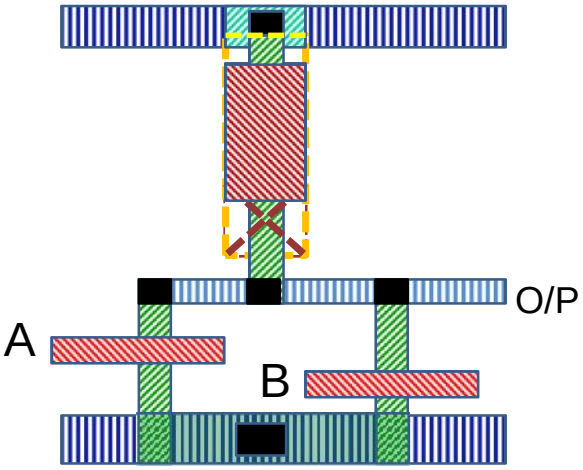
4:1 nMOS inverter

LAYOUT DIGRAM FOR nMOS

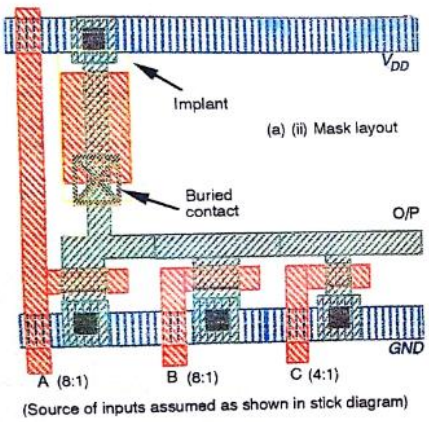


2 input nMOS NOR gate

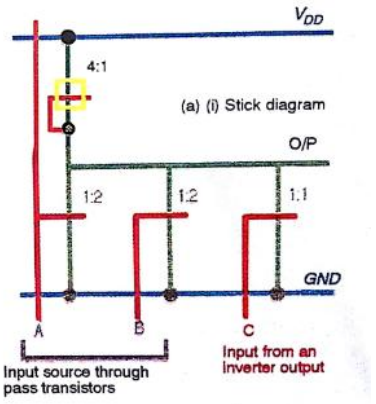




Stick diagram and Layout nMOS 3 input NOR gate

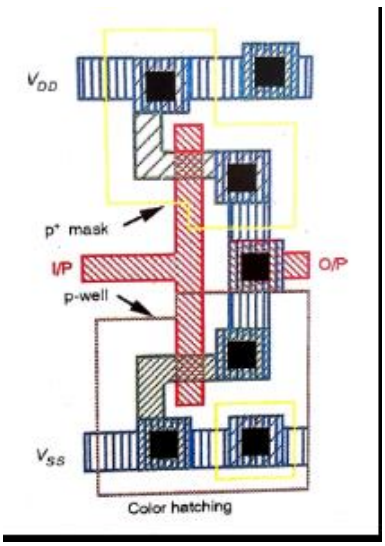


(Source of inputs assumed as shown in stick diagram)



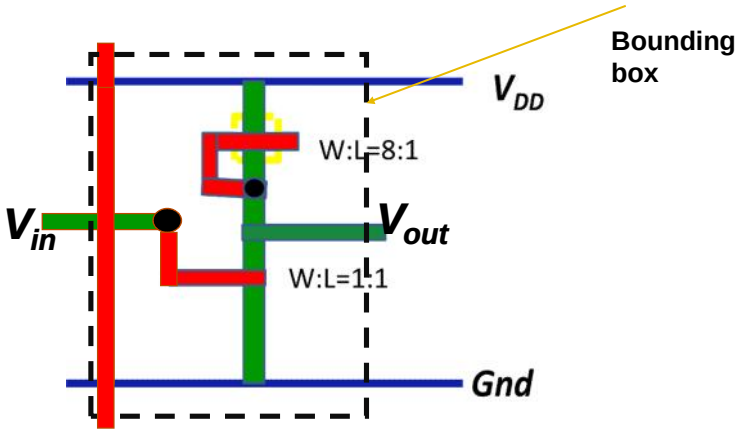
Stick diagram –CMOS inverter

Layout –CMOS inverter

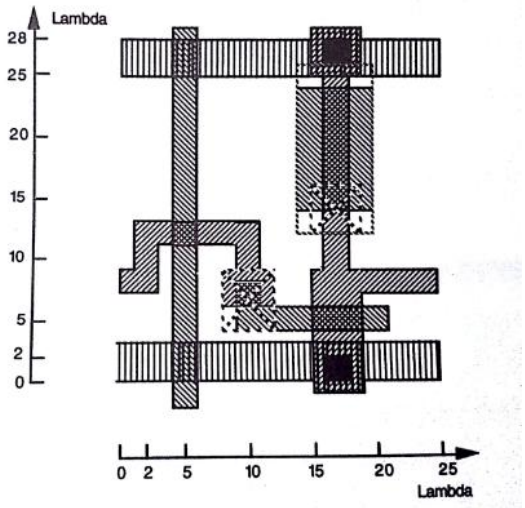


Shift register cell with nMOS

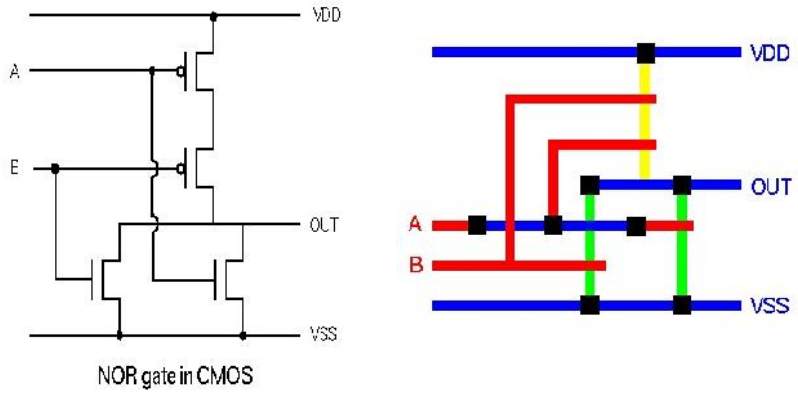
- propagate the control signals at right angle on poly



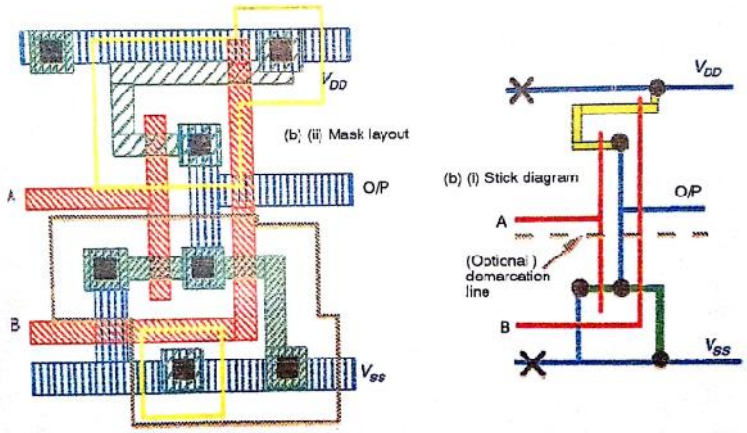
Layout of nMOS shift register cell



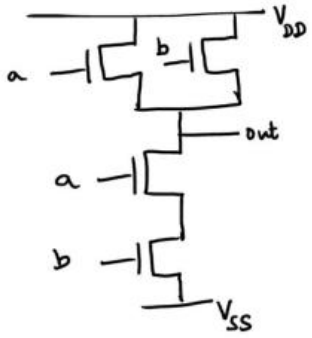
Stick Diagram- 2 input CMOS NOR gate

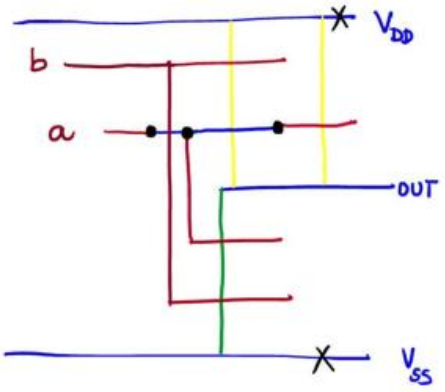


Stick Diagram and Layout of two input CMOS (p-well) NOR gate



Stick Diagram – 2 input CMOS NAND gate

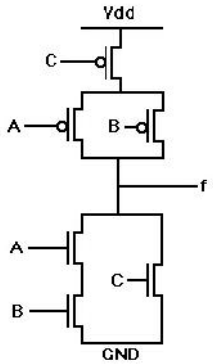


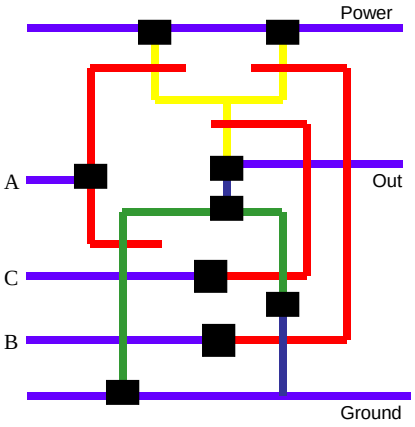


Exam questions- 3 input NAND,NOR stick diagrams (practise)

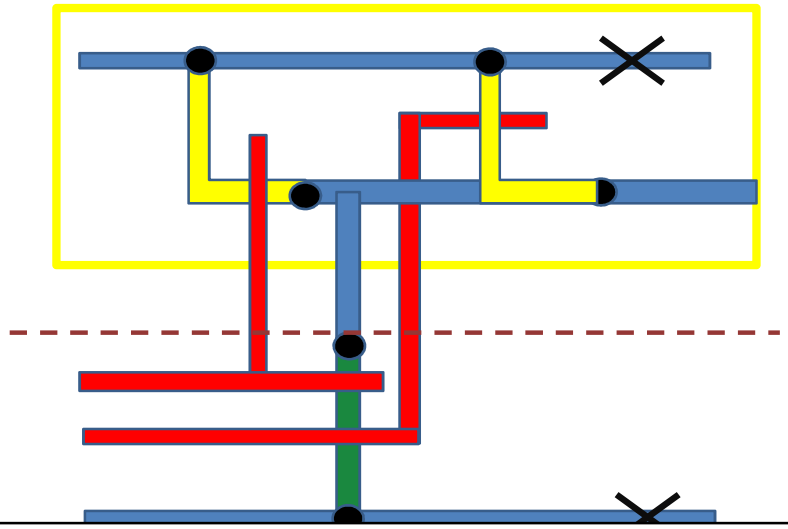
Stick Diagram-Example

Example: $f = \overline{(A \bullet B) + C}$

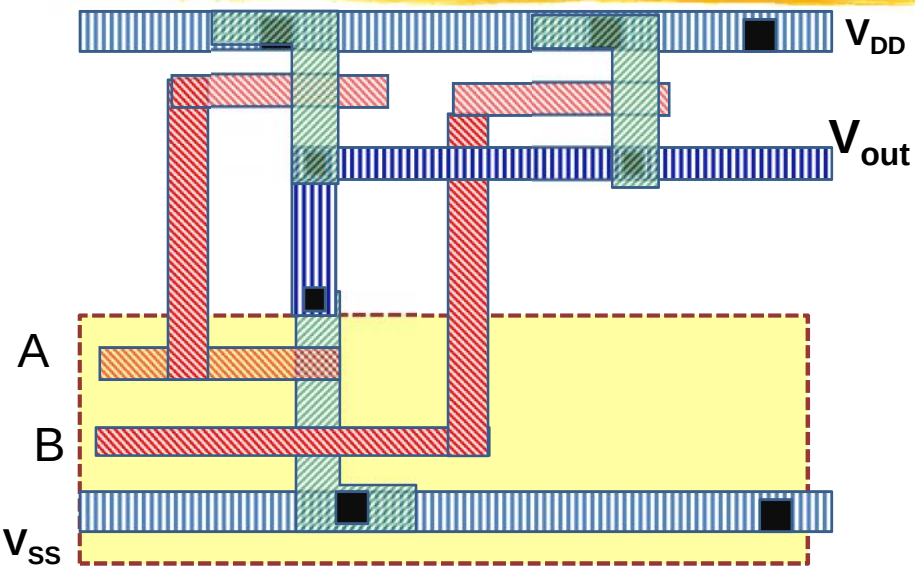




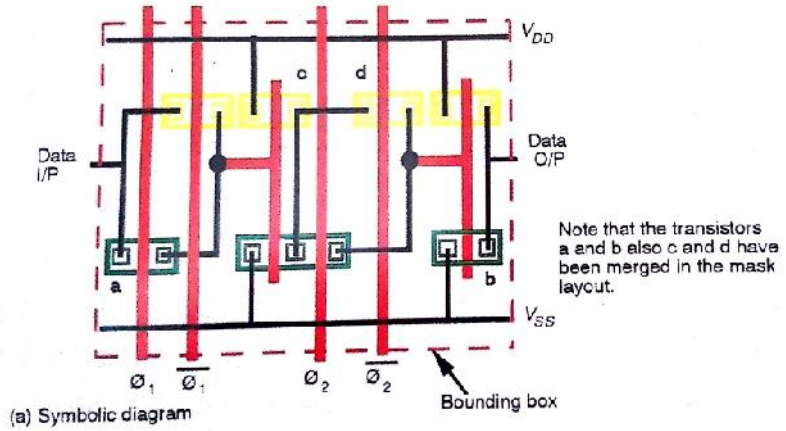
2 input CMOS NAND GATE



LAYOUT OF 2 input NAND GATE

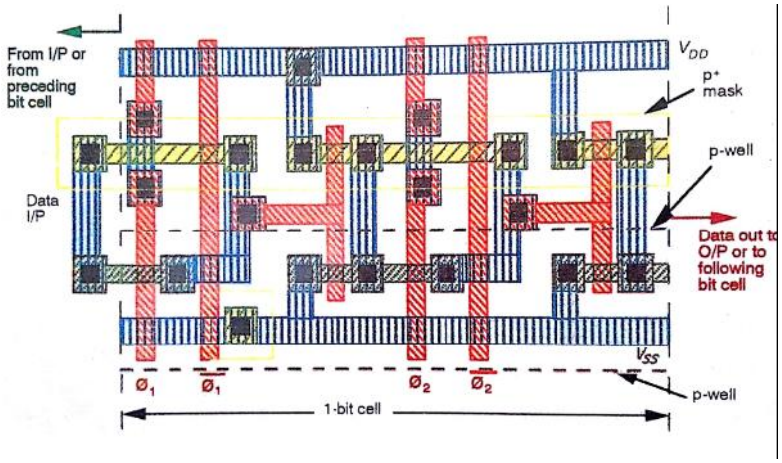


Stick Diagram- 1 bit CMOS shift register



(a) Symbolic diagram

Stick Diagram- 1 bit CMOS shift register



Lambda based Design rules

- Most foundry allows submission of designs using simpler set of design rules that can be easily scaled to different processes.
- These are called “lambda design rules” λ that has units of µm.
- All distance and widths and spacing are written as

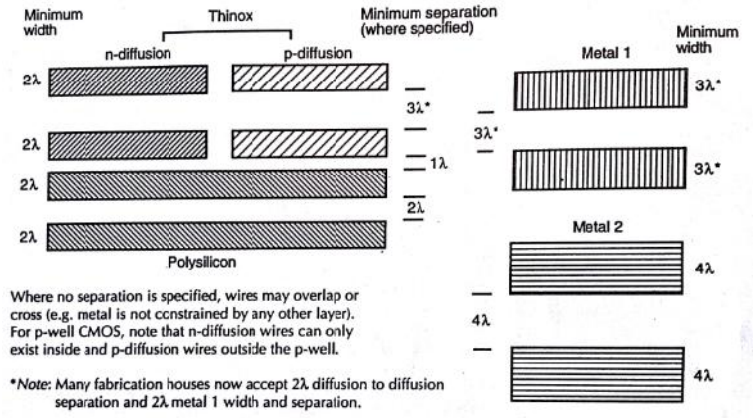
  value = mλ, where m is scaling multiplier.

  for ex.: w =3 λ, L= 4 λ

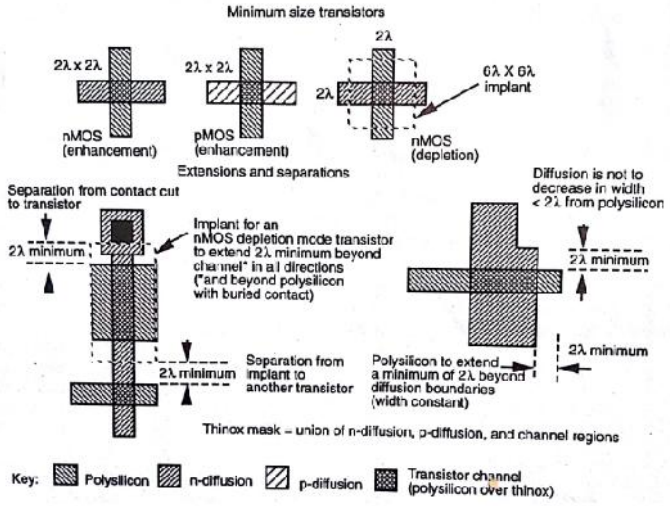
If the factory will use technology λ=0.15 µm

w =0.45 µm, L = 0.6 µm

Design rules for wires



Design rules for Transistors



CONTACT CUTS

Contact between polysilicon and diffusion

1. Poly to metal and then metal to diffusion.
2. Buried contact polysilicon to diffusion.
3. Butting contact (Poly to diffusion using metal).

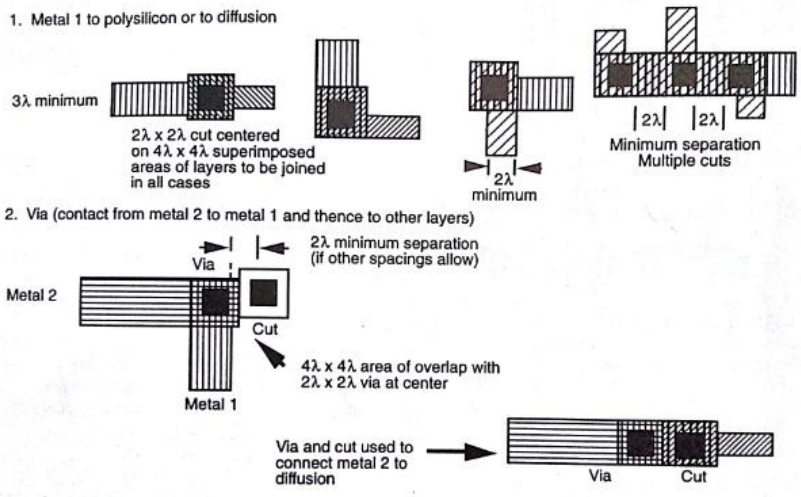
Buried contact is most widely used, occupies less area and reliable contact.

Via connections- using metal as intermediate material.

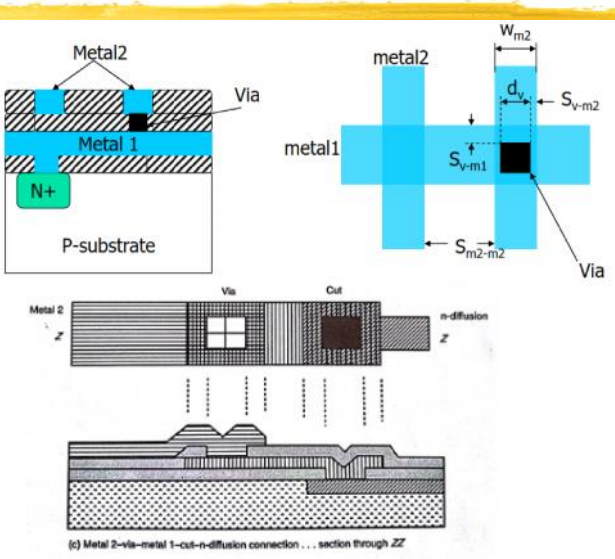
Connection between metal and Polysilicon/diffusion

- 2λ X 2λ contact cut indicates the area in which oxide is removed down to undelying polysilicon or diffusion surface.
- When deposition of metal take place it is deposited through the contact cut areas so that connection is made between the two layers.
- Via cut is used for connecting from metal2 to metal 1 and then to diffusion/polysilicon.

CONTACT CUTS

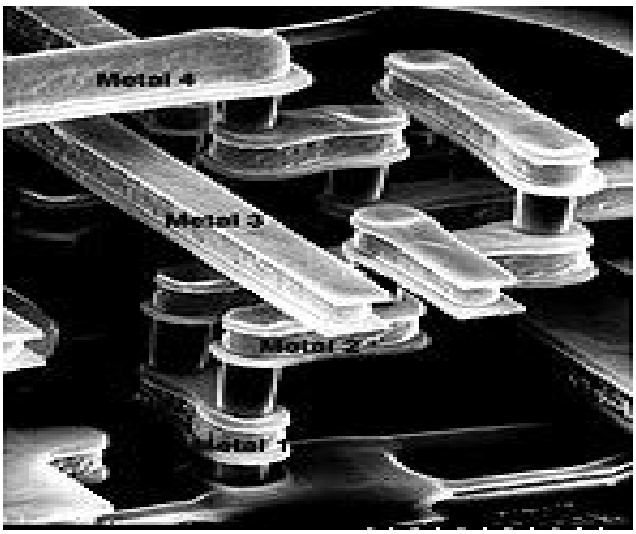


Via Cut

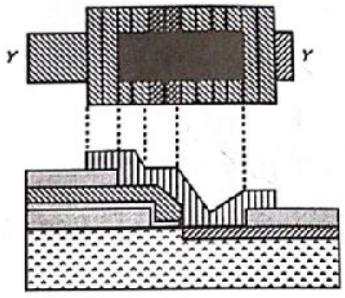


Metal 2 –Via Metal 1-cut-n-diffusion connection

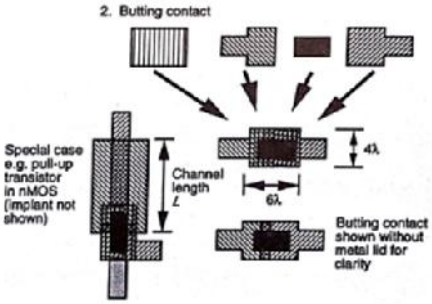
Via Cut



Diffusion to polysilicon using butting contact approach

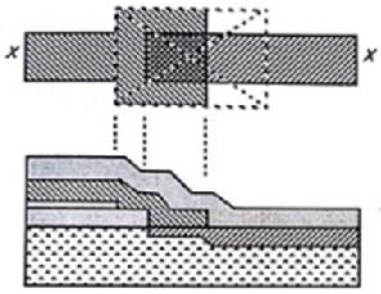


(b) Butting contact . . . section through *YY*



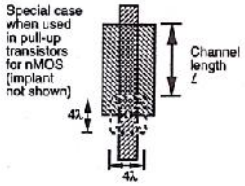
- 2λ X 2λ contact cut is made down to each of the layers to be joined.
- The layers are butted together that the contact cuts becomes contigious.
- The polysilicon and diffusion layers are also butted together.
- Contact between butting layers is made by metal overlay.

Buried contact-Polysilicon to diffusion



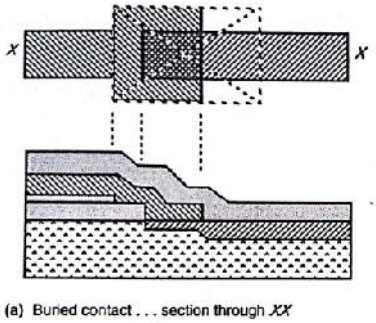
(a) Buried contact . . . section through *XX*

- Layers are joined over a 2λ X 2λ area with buried cut extending 1 λ in all directions around the contact area.



- Contact cut extension is increased to 2 λ in diffusion paths to avoid forming unwanted transistors.

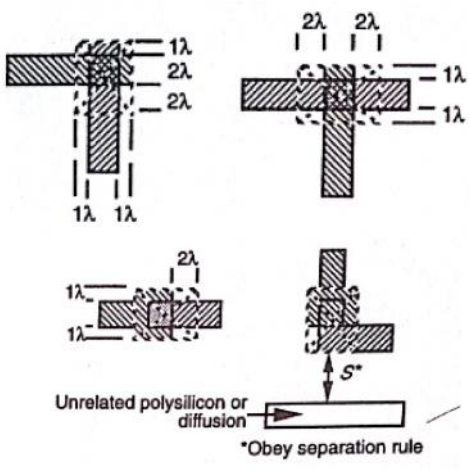
Buried Contact



(a) Buried contact . . . section through XX

- Layers are joined over a 2λ X 2λ area with buried contact cut extending by 1λ in all directions around the contact area except that the contact cut is increased to 2λ in diffusion paths leaving the contact area .This is to avoid forming unwanted transistors.
- Buried contact is smaller in area than butting contact.

Buried Contact

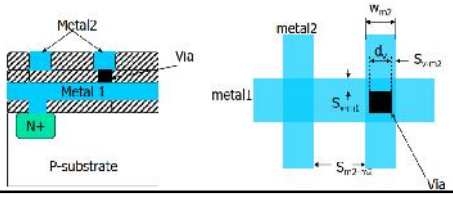


Double metal MOS process Rules

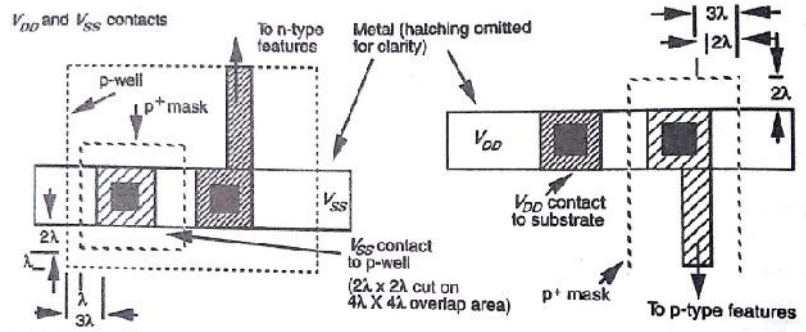
- A second metal layer is added to the previous process.
- Used for global distribution of V_{DD} and V_{SS} and clock lines.
- First metal layer is used for local distribution of signals and power.
- Second layer metal layer is coarser(harder and harsh) than first level metal layer.
- Oxide layer is thicker between first and second layer metal lines.
- Layout rule- both metal layers sholud be orthogonal to each other.

Process

- Oxide below first metal layer is deposited by CVD(chemical vapor deposition process.
- Oxide layer between metal layers is also deposited by CVD.
- Selected areas of oxide are etched by plasma etching.
  (high level of vertical ion bombardment to allow for high and uniform etch rates)
- Second metal is deposited to form a via and metal line as well.

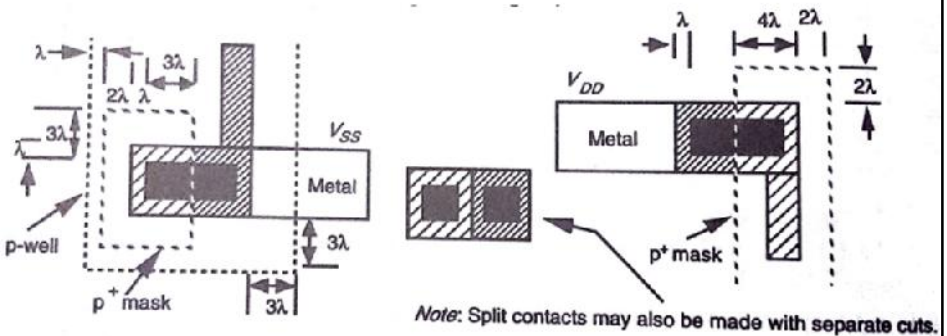


CMOS LAMBDA BASED DESIGN RULES



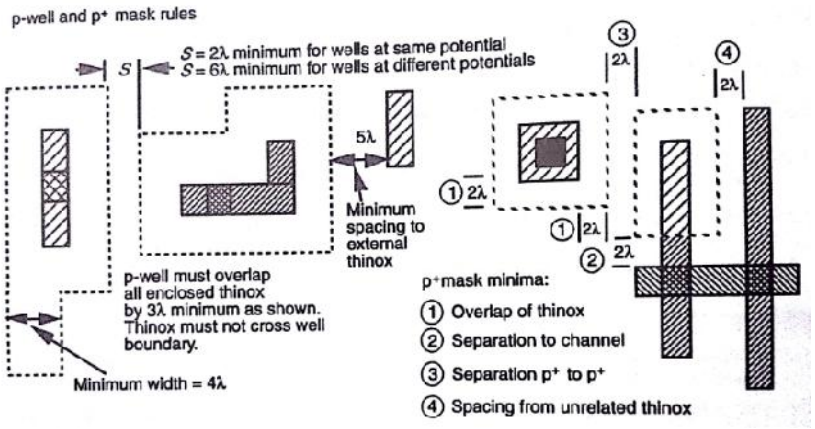
Each of the above arrangements can be merged into single 'split' contacts.

CMOS LAMBDA BASED DESIGN RULES



Note: Split contacts may also be made with separate cuts.

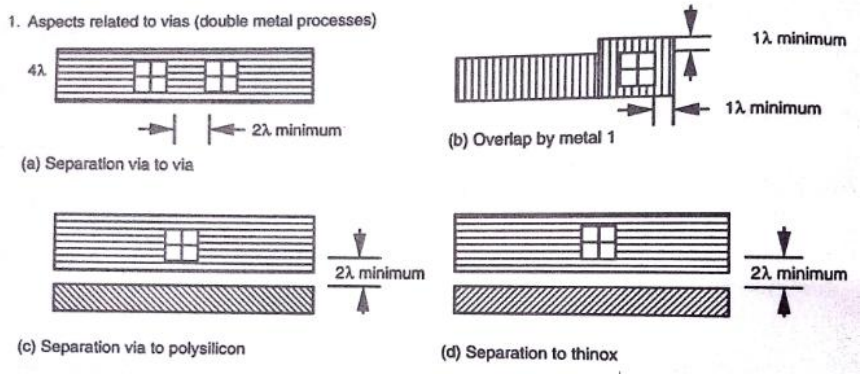
CMOS LAMBDA BASED DESIGN RULES



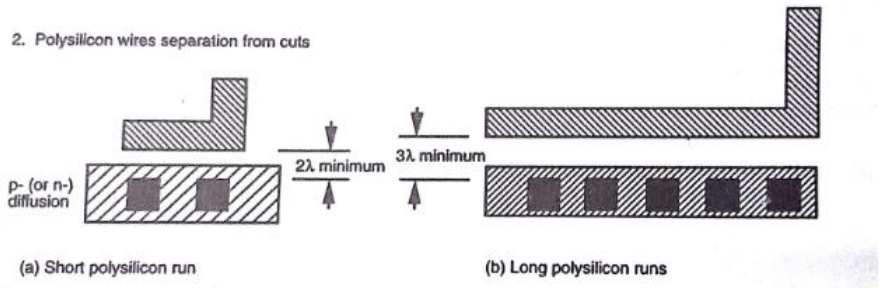
GENERAL OBSERVATIONS ON THE DESIGN RULES

- The goal of any set of designed rules should be to optimise the yield while keeping the geometry as small as possible without compromising the reliability of the finished circuit.
- If line widths are too small, they become discontinuous after certain length.
- If separate paths are placed too close ,they might merge at certain places or interfere(signal interference) with each other.
- λ should include errors also (only on width dimension allowed).

λ based design rules for contacts for higher yield /reliability



λ based design rules for contacts for higher yield /reliability



λ based design rules for contacts for higher yield /reliability